Integration Technologies for 3D Systems

A. Klumpp, P. Ramm, R. Wieland, R. Merkel

Fraunhofer Institute for Reliability and Microintegration,
IZM-Munich; 3D
IZM-Berlin; Electroplating

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(01M2926 D/E & 01M2999/A)

Outlook

- Introduction
- Handling Concept
- Basic Technologies
- Relevant Technological Integration Concepts
- Stack Formation Results
- Summary
- Conclusion

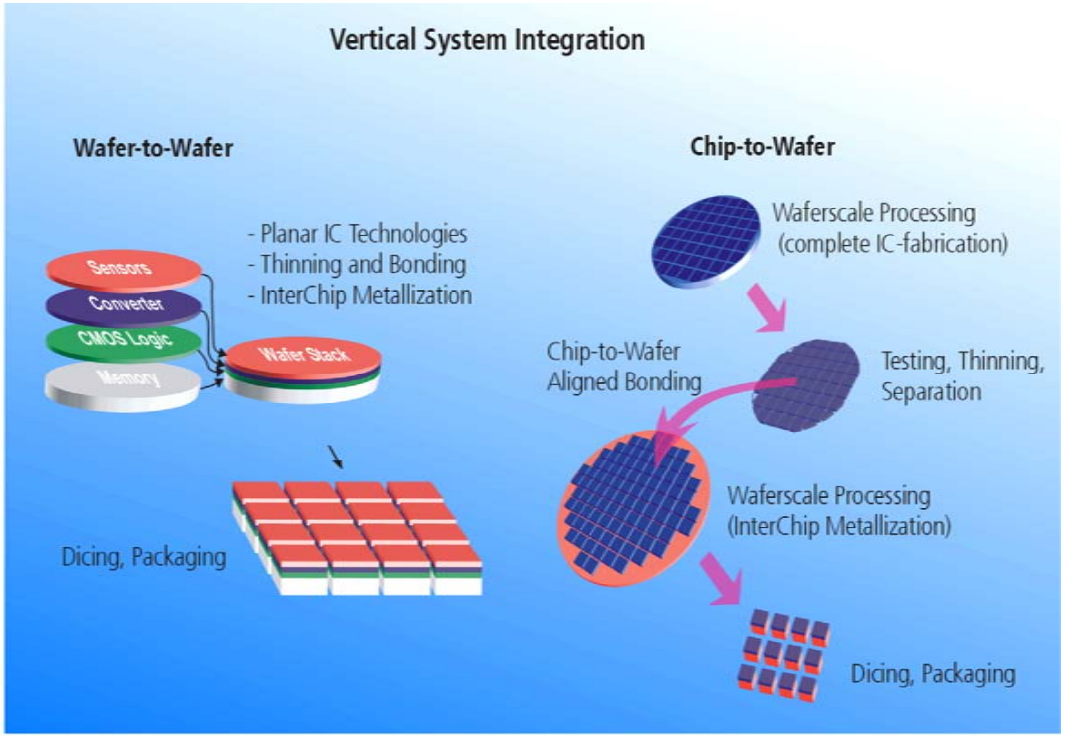
Key Applications and Potential of 3D

- Mobile Systems

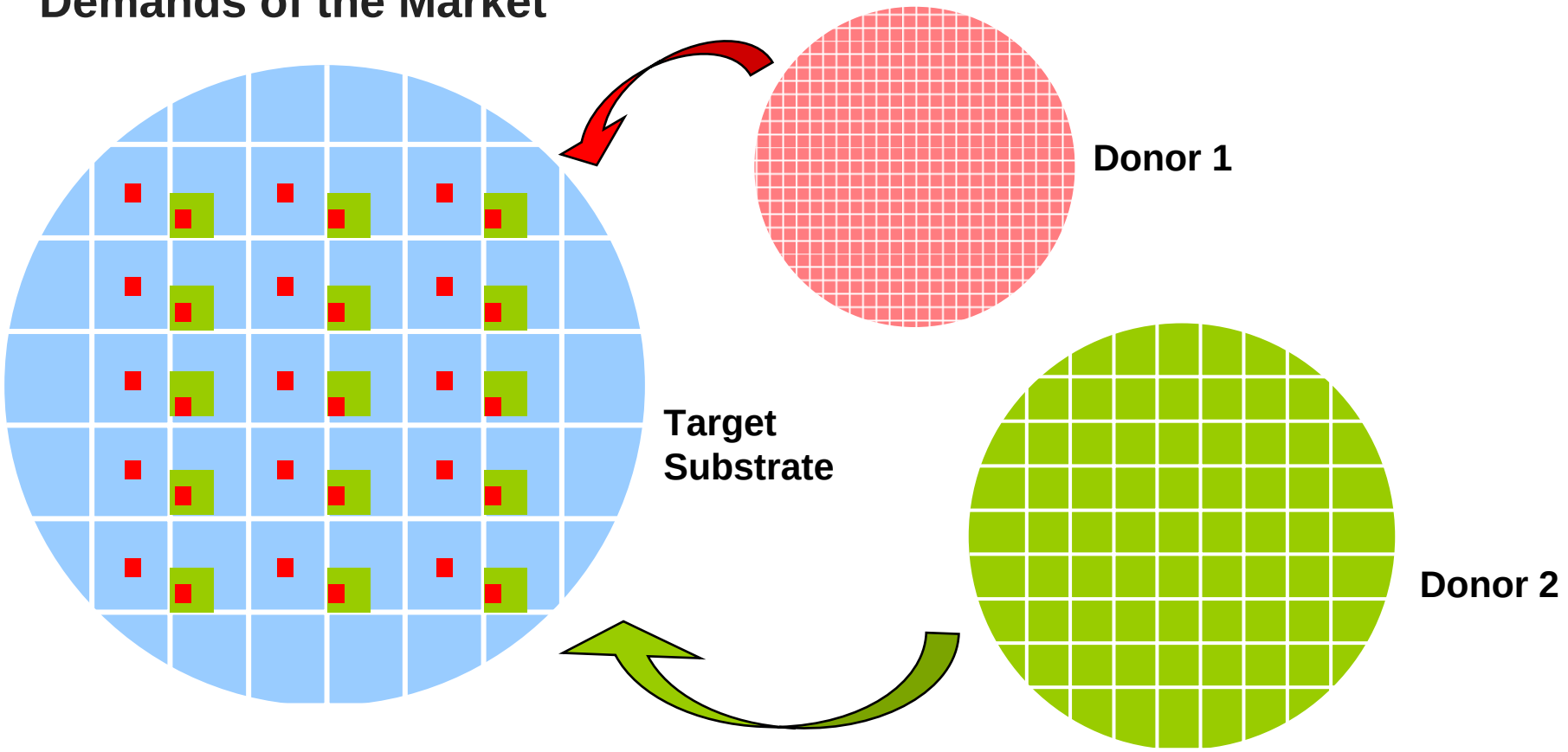
  (minimum volume, low power, security)
- Systems for high parallel signal processing

  (e.g. image sensor)

- Increased Integration density
- More Functionality
- Mixed Technologies: 3D SoC



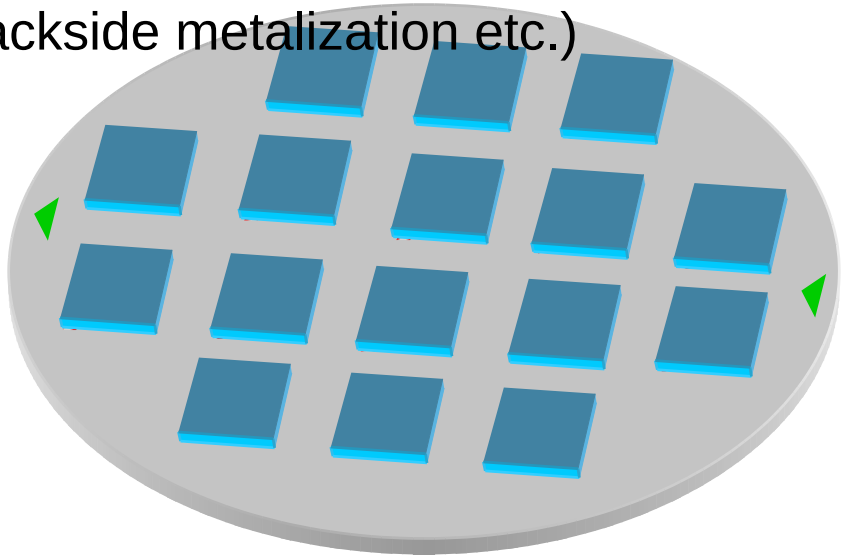
Demands of the Market



Handling Concept

Handling Concept for Wafer-Level Chip-Scale Processing (1)

- Placement of Chips on Handling Substrate
  - Grid of Aligment Marks according to the Positions on the Target Wafer
- Processing of Chips on Wafer Scale
  (e.g. cleaning prior to bond, thinning, backside metalization etc.)



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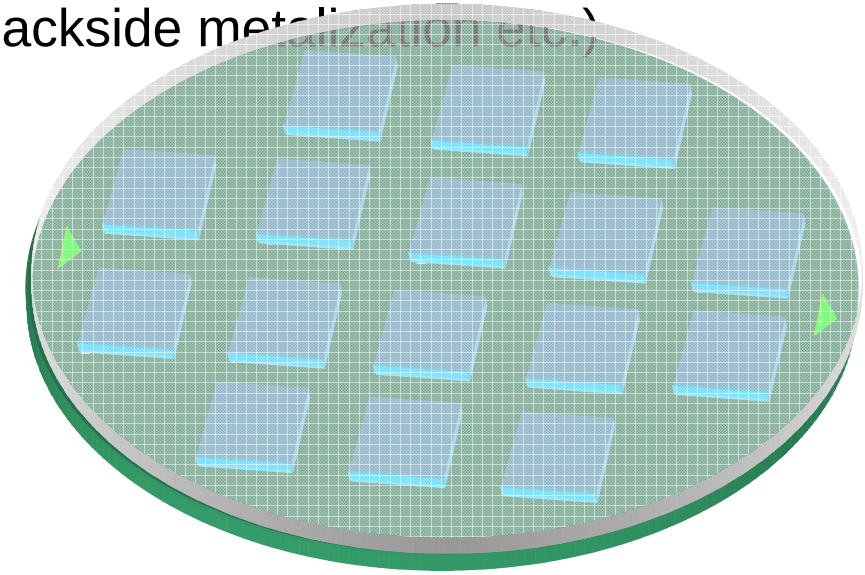
- Transfer to Target Wafer
  - Adjusted Stack Formation (Wafer-Flip)
  - Removal of Handling Substrate



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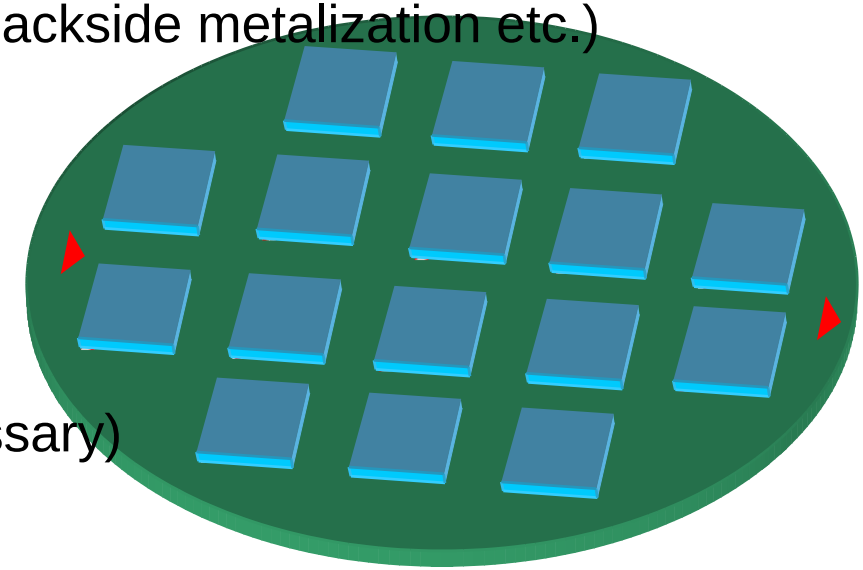
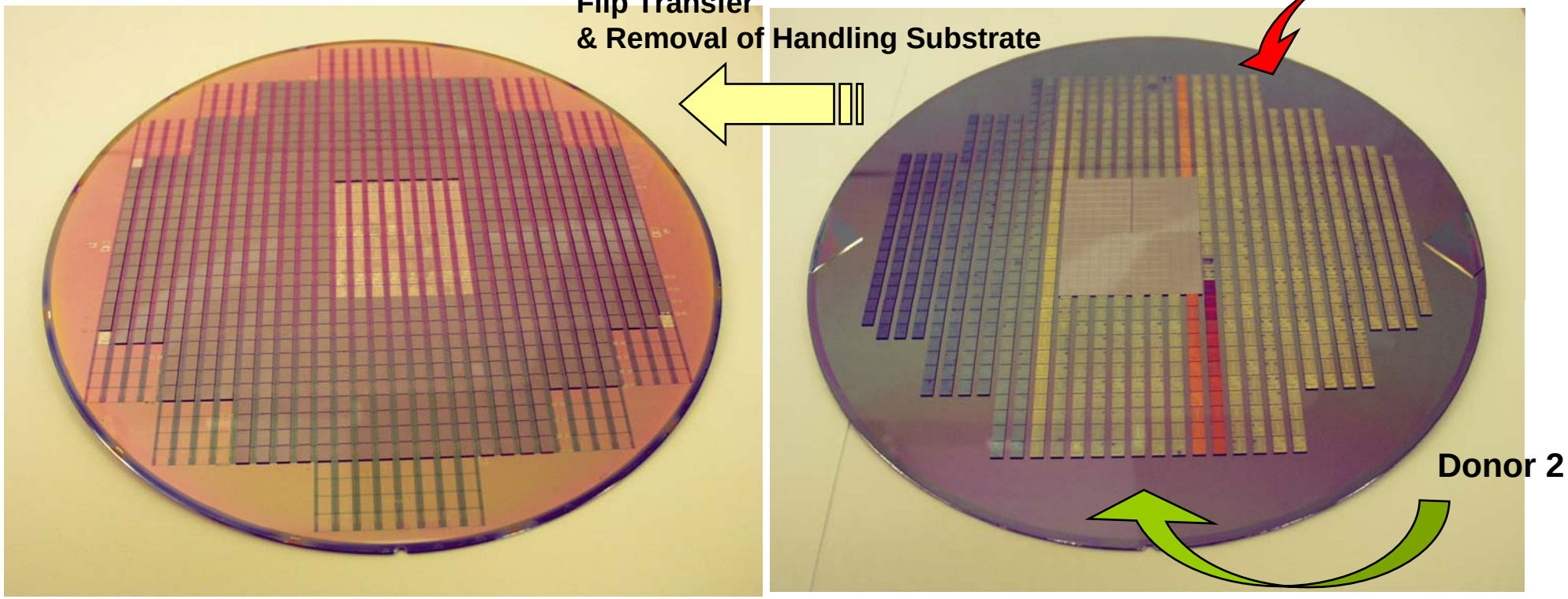
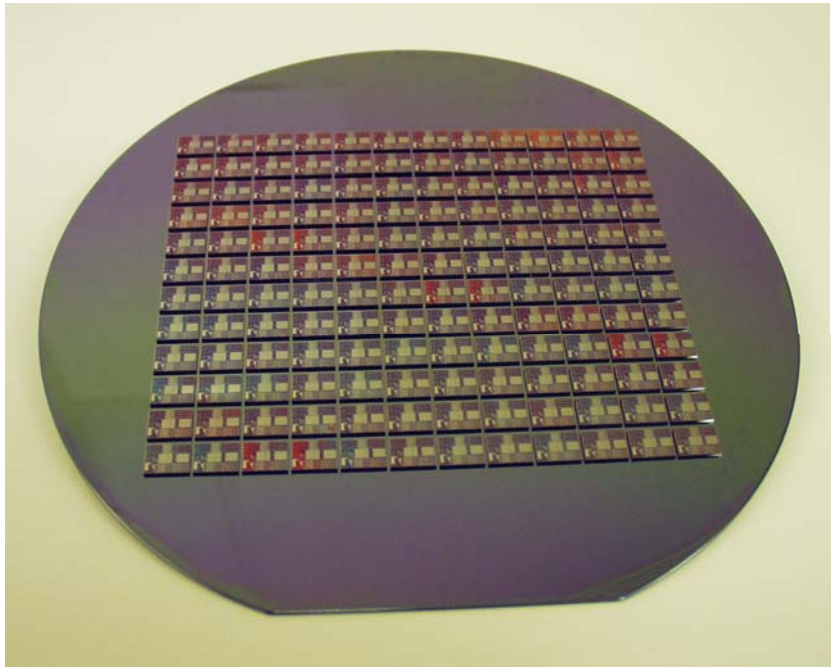
- Transfer to Target Wafer
  - Adjusted Stack Formation (Wafer-Flip)
  - Removal of Handling Substrate
- Further Processing of new Stack (if necessary)



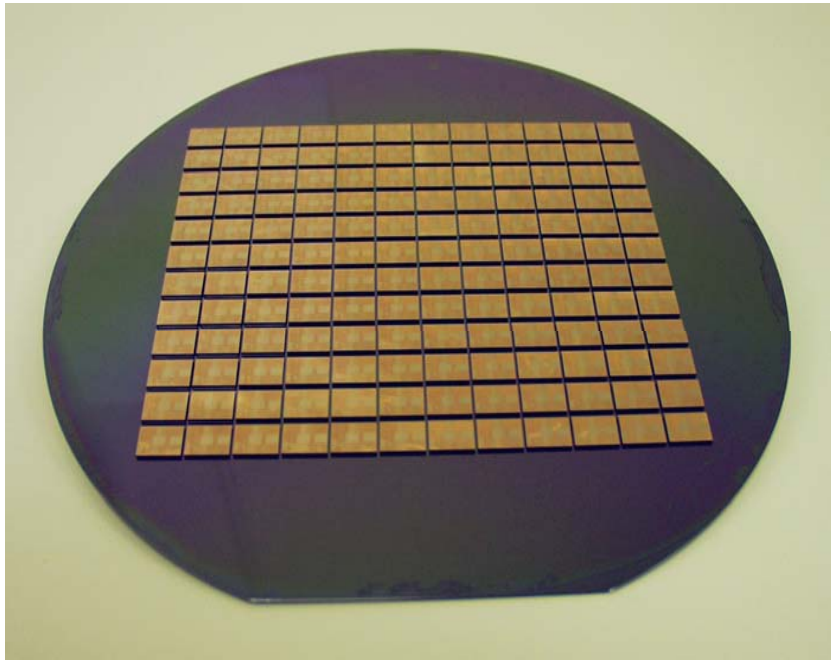
Handling Concept WL-CS (2)



Handling Concept WL-CS (3) Removal of Copper Oxide



**Chips on Handling Substrate;
blue colour of chips results from copper oxide formation during placement procedure**



Clean copper surface after wet chemical removal of copper oxide (wafer or batch)

Basic Technologies

Wafer Thinning Technology at IZM, Munich

Handling concepts for thin wafers
substrate thickness: 150 … 70 µm

Carrier substrates for handling of ultra-thin wafers
substrate thickness: **50 … 10 µm**

Reversible Mounting techniques:
thermoplastic materials, wax, adhesive tapes, resist, high temperature carriers

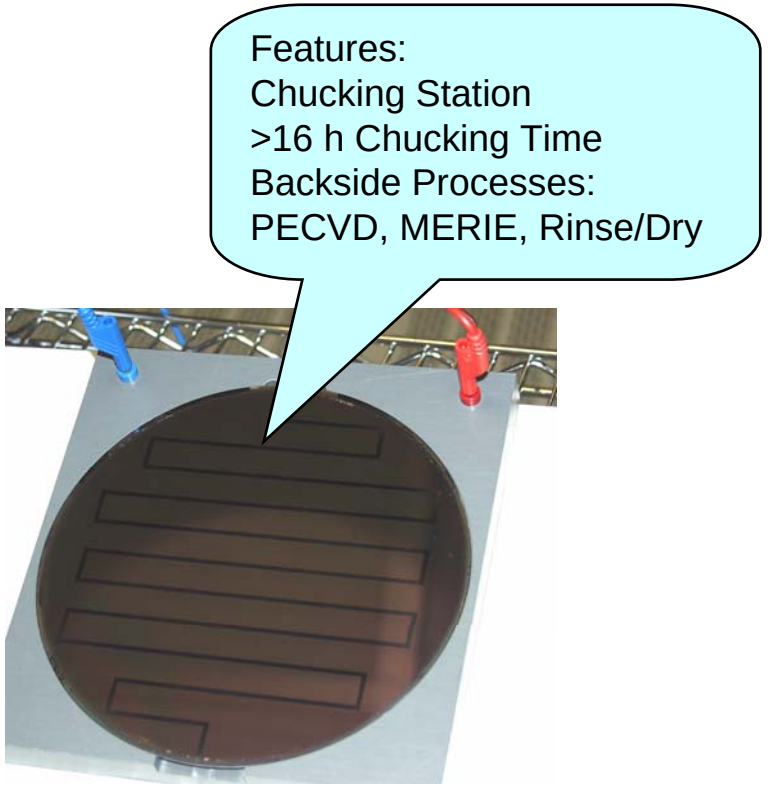
Wafer thinning
grinding (DISCO DFG 850), spin-etching (SEZ SP 203), CMP polishing (LAM, Westech), Plasma dry etching

Dicing technology: **Dicing-by-Thinning concept** “DbyT”
uses dry etched chip trenches for stress-free separation of ultra-thin ICs

Development of **complete process flow**: from rigid wafers to packaged thin devices

Low Cost Handling Concept: E-Chuck Si-Wafer, reusable

- **Prototype Electrostatic Chuck successfully tested (200 mm)**
- **Chucking Principle: Bipolar electrostatic**
- **Built on Si-Wafers, CMOS compatible**
- **Chuck-Wafer Thickness: 100 µm < d < 720 µm**

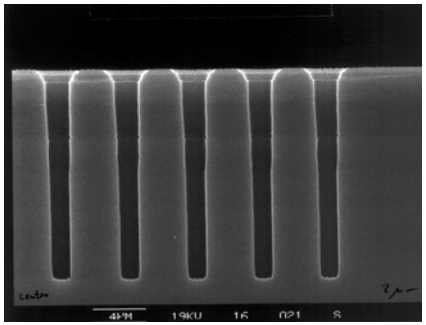


Electrostatic-Chuck (3)

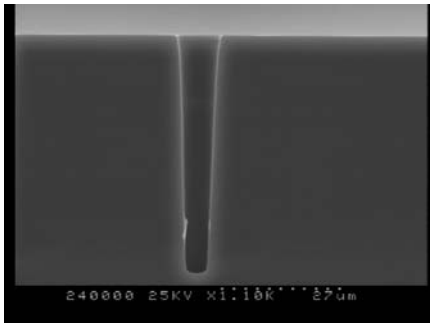
e-Chuck action: thin sample on chuck, without (left) and with (right) applied voltage

Via Formation for VSI – *Via Etching*

1.0	2.0	3.0	5.0	10	100	Via-Diameter [µm]



16 µm,
8:1



40 µm,
4:1

Etch Capability
IZM-M

10	16	20		40	60	70	Via-Depth [µm]
10:1	8:1	7:1		4:1	6:1		Aspect Ratio

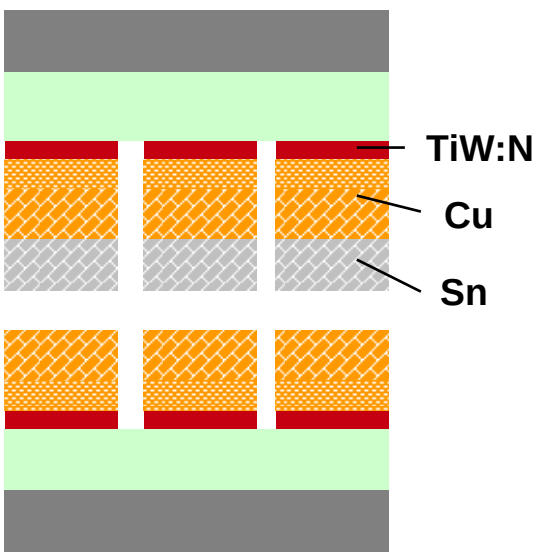
Via Formation for VSI – *Via Metal Filling*

1.0 µm	3.5 µm	5 µm	10 µm	....	100 µm	Via-Diameter

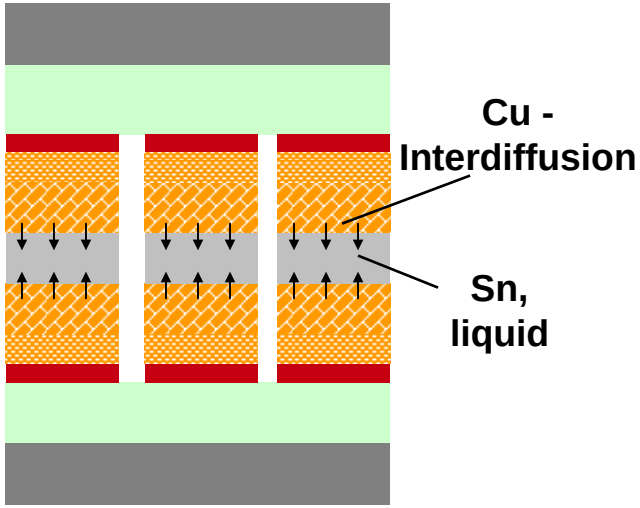
CVD of - copper - tungsten - TiN	Electroplating of - copper PVD of Seedlayer - Ti:W / Cu	Process for filling

10 µm				70 µm	....	100 µm	Via-Depth
10:1	3:1	2:1	..	7:1		1:1	Aspect Ratio

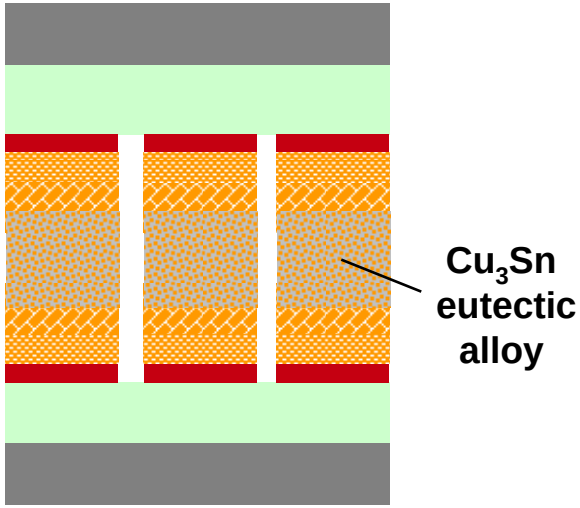
Metallization SLID (Solid Liquid Interdiffusion)



Through Mask Electroplating



Contact under Pressure and Heat
~ 5 bar, 260 – 300 °C (Sn-melt)

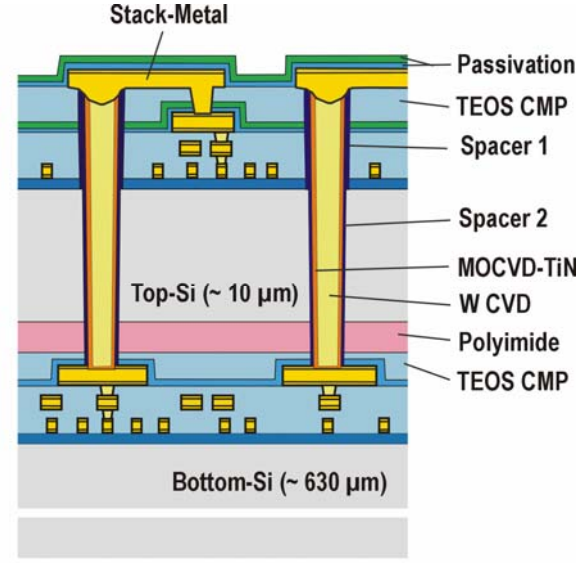


Formation of Eutectic Alloy;
T_{melt} > 600 °C

Integration Concepts and Realization

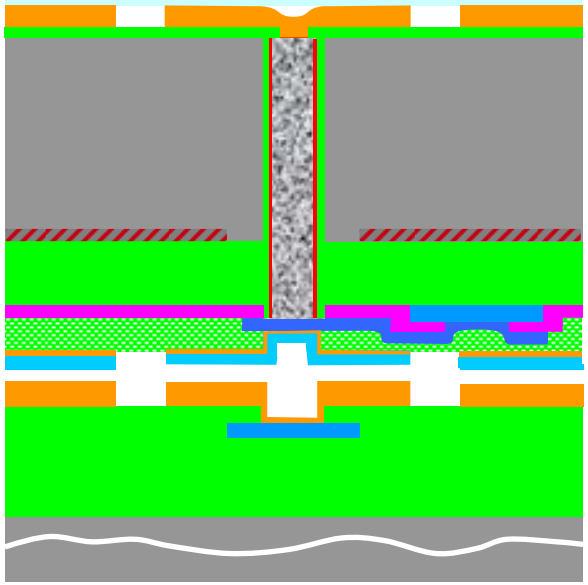
Vertical System Integration – *Three relevant Concepts (IZM-M)*

InterChip Via (ICV)



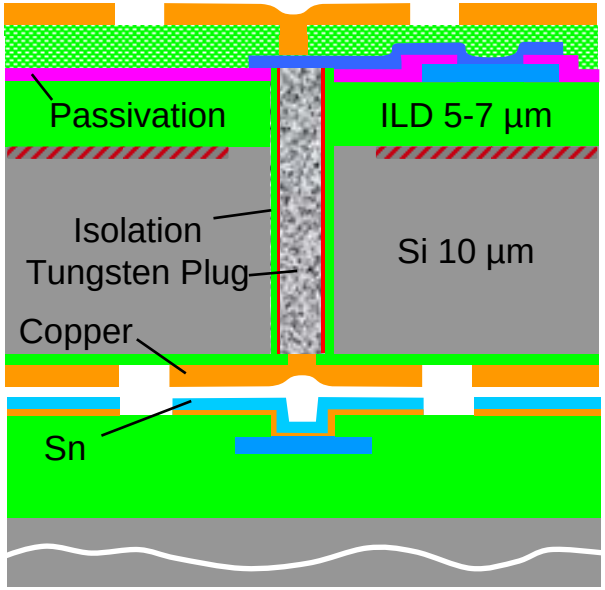
W-Plug / Polyimide

Face to Face modular (F2F-M)



W-Plug / Cu / Sn

ICV / SLID



W-Plug / Cu / Sn

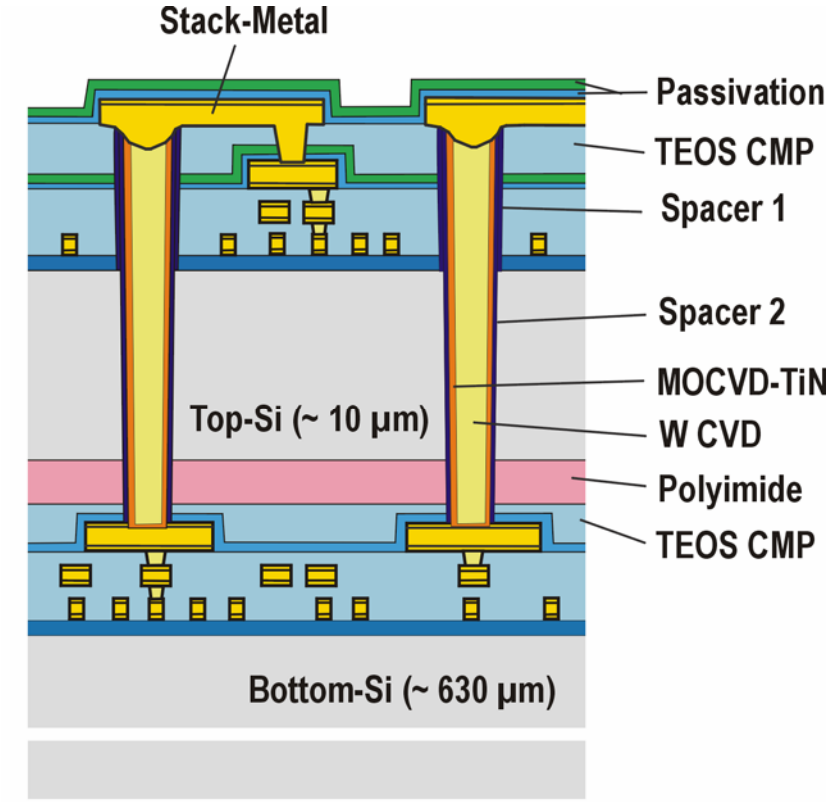
Two Layer Stacks with

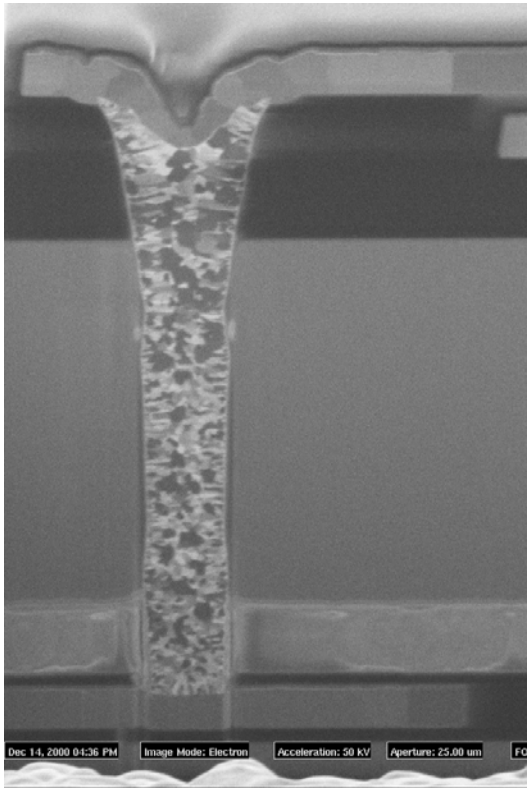
ICV (Polyimide based)

and

InterChip Via / Slid (Metal based)

ICV Stack *(FIB; Tungsten)*





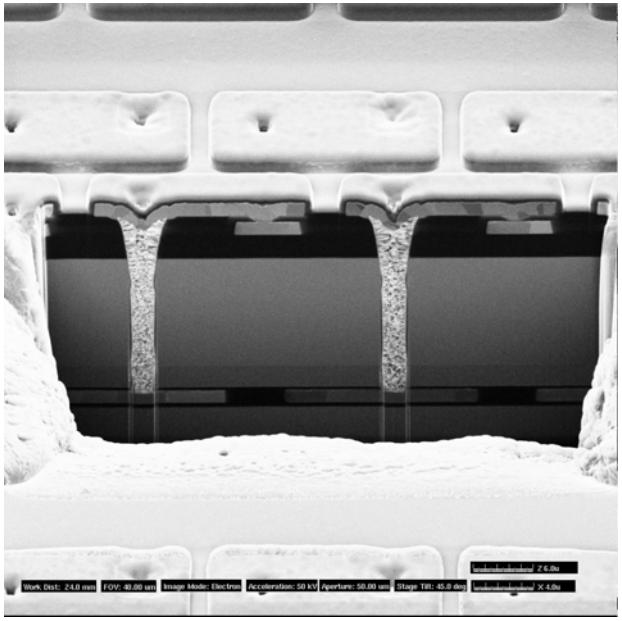


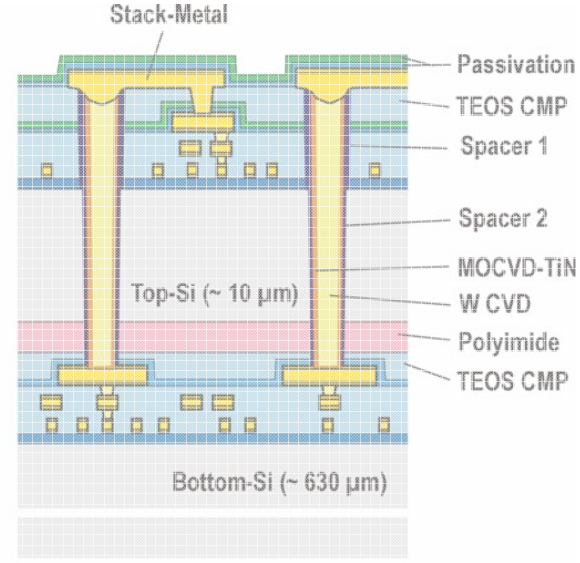
Fig.: Cross section of a vertically integrated test chip structure, showing 2.5 x 2.5 µm² interchip vias (FIB)

WL-CS-3D – *Three layer stack (0)*

Three Layer Stack with Face-to-face Modular

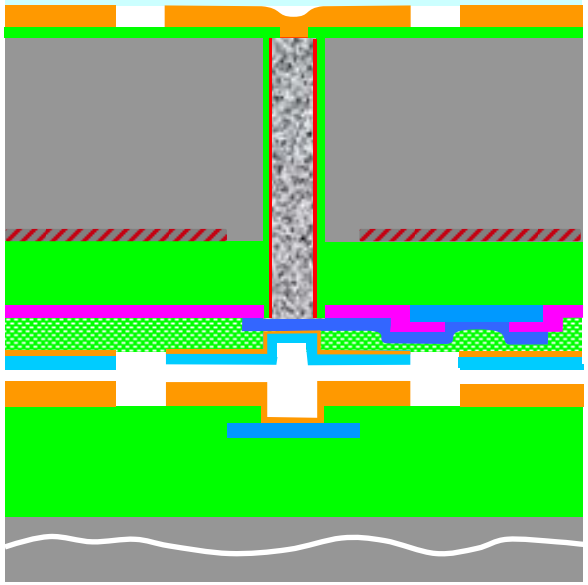
Vertical System Integration – *Three relevant Concepts (IZM-M)*

InterChip Via (ICV)



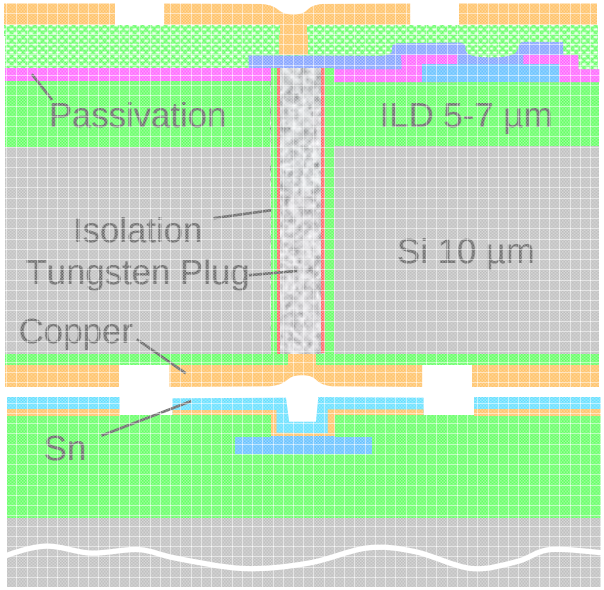
W-Plug / Polyimide

Face to Face modular (F2F-M)



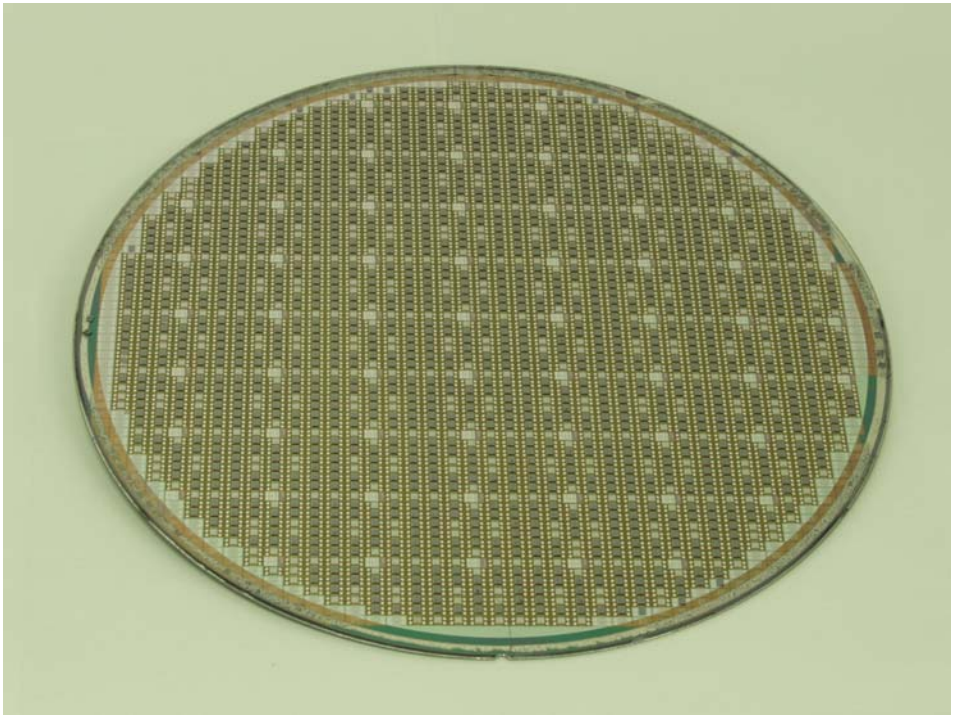
W-Plug / Cu / Sn

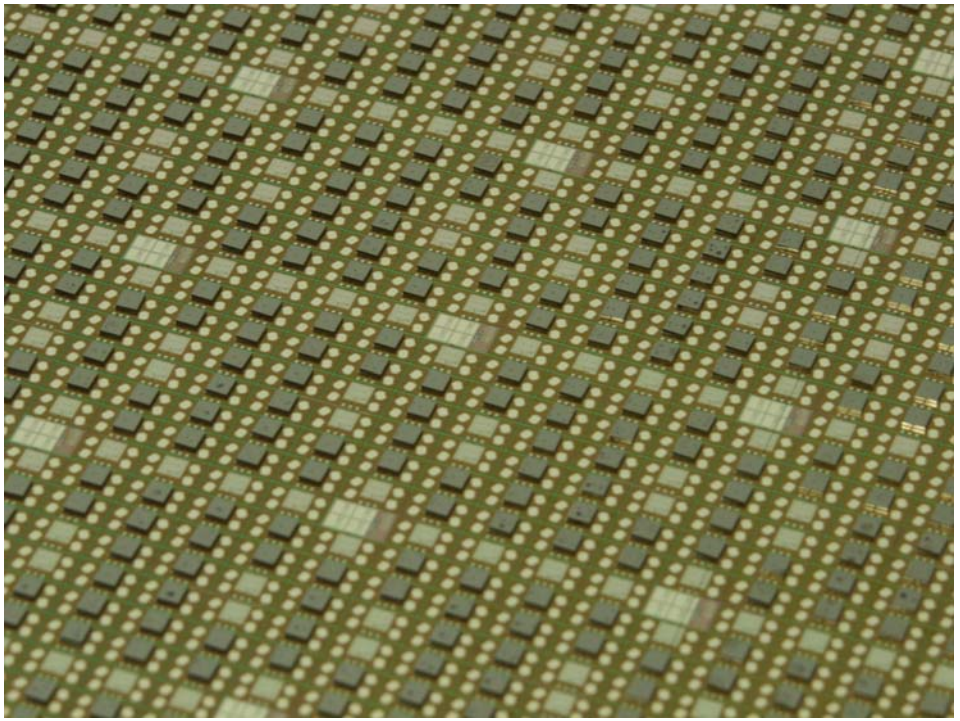
ICV / SLID



W-Plug / Cu / Sn

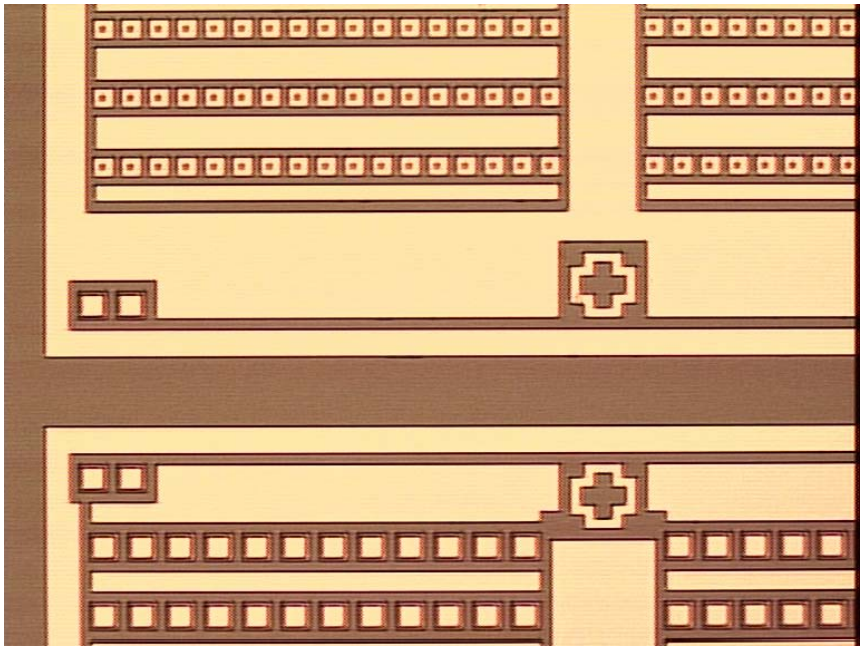
VSI by Soldering: „SLID Technology“ (2)

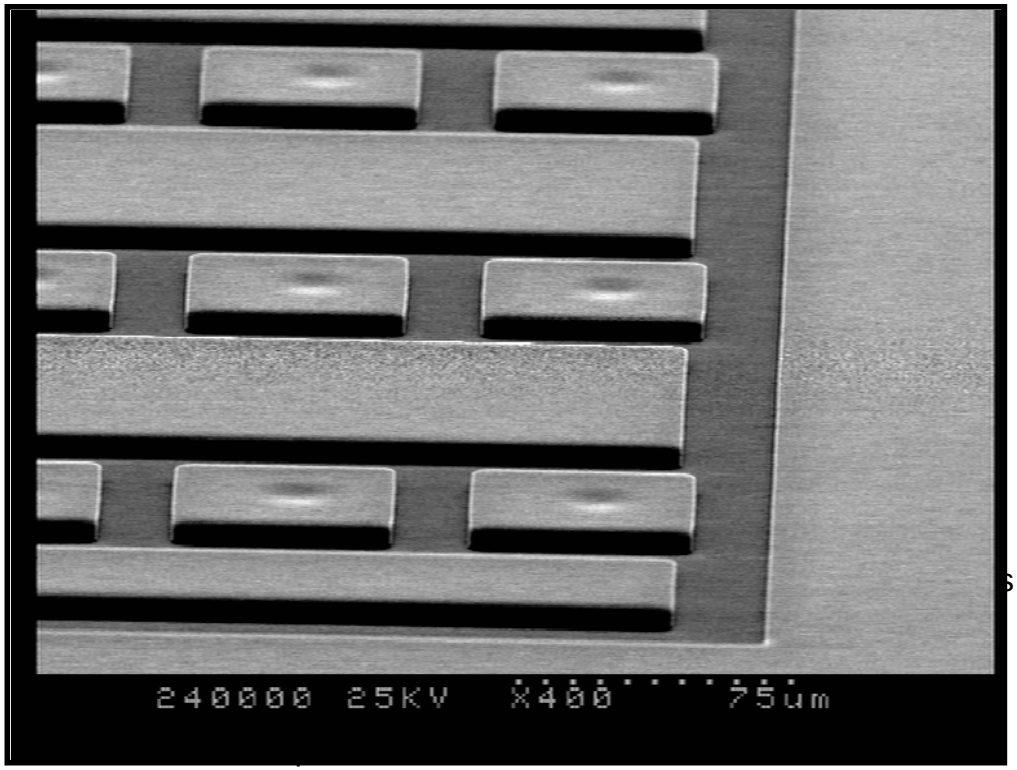




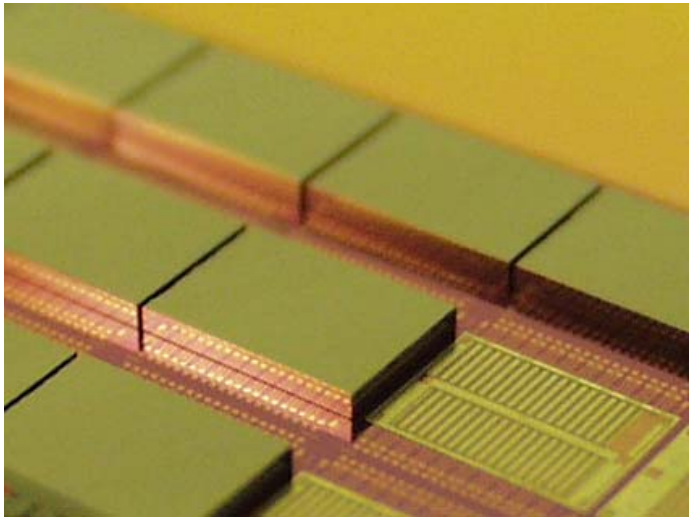
Example of Infineons Application of SLID for Products

Metallization SLID - *Trough Mask Electroplating (2)*
Testchip for F2F-M & ICV/SLID

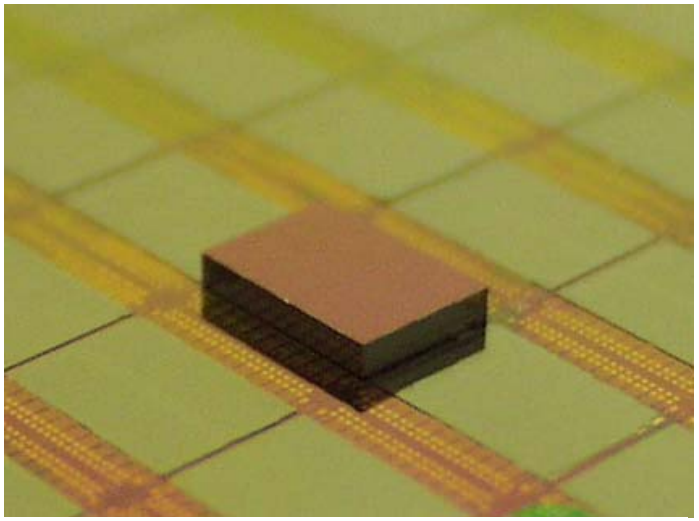




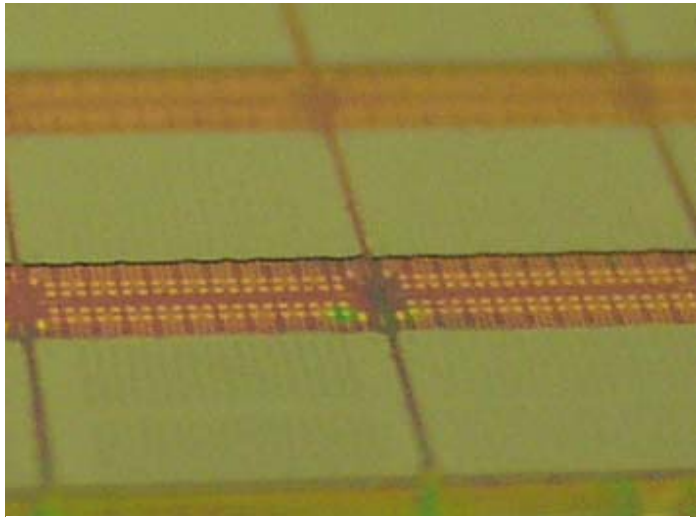
WL-CS-3D – *Three layer stack (1)*



C2W-Transfer Development
After Chip Transfer from Intermediate Handling Wafer to Target Substrate
Chip Thickness 500 µm



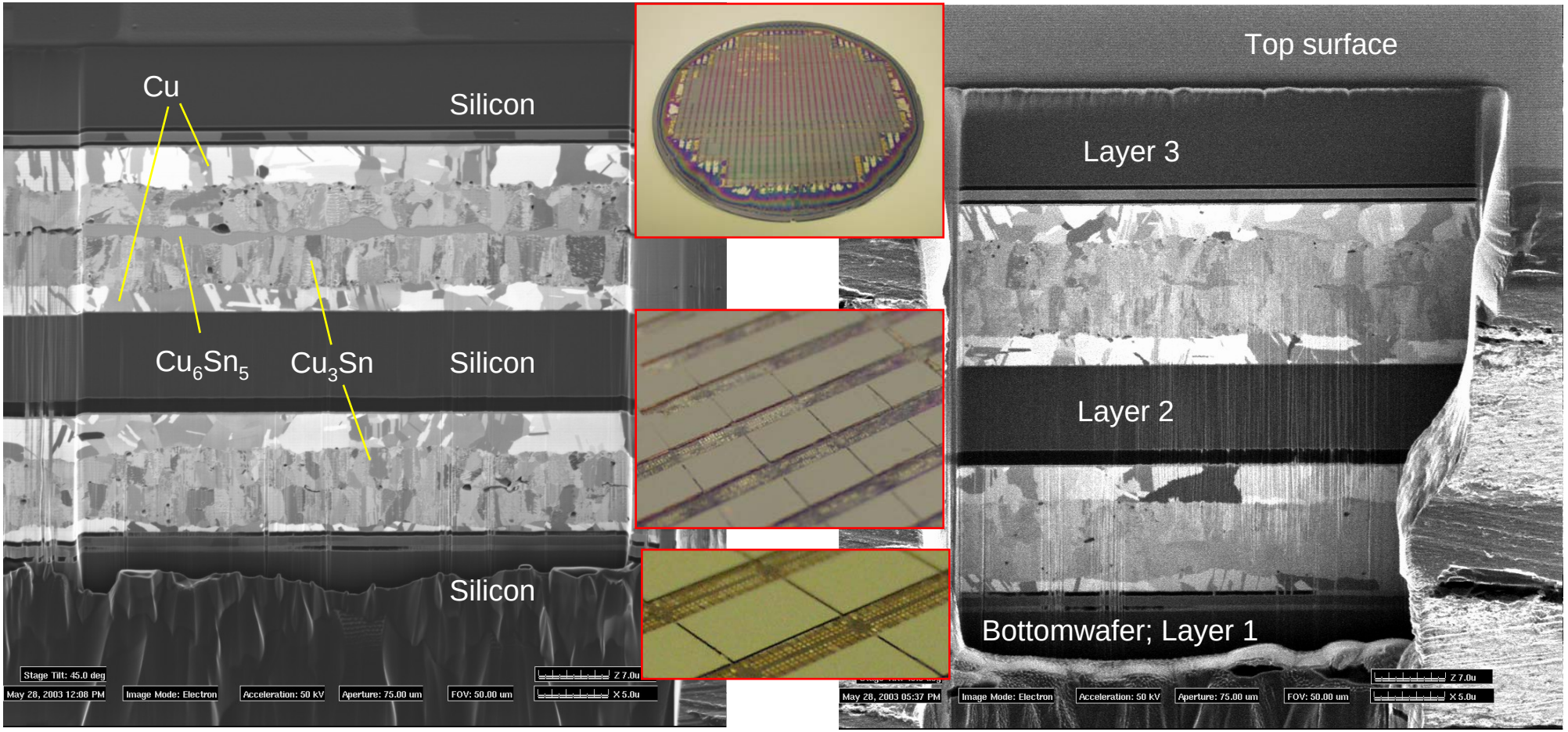
After Thinning on Target Substrate
Chip Thickness 10 µm
plus original Chip for Comparison



After Thinning on Target Substrate
Chip Thickness 10 µm

Measured Resistance with Daisy Chain Structure:
0.5 Ohms / Contact (incl. 2 Diffusion Barriers)

3D System Integration



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WL-CS-3D – *Three layer stack (5)*

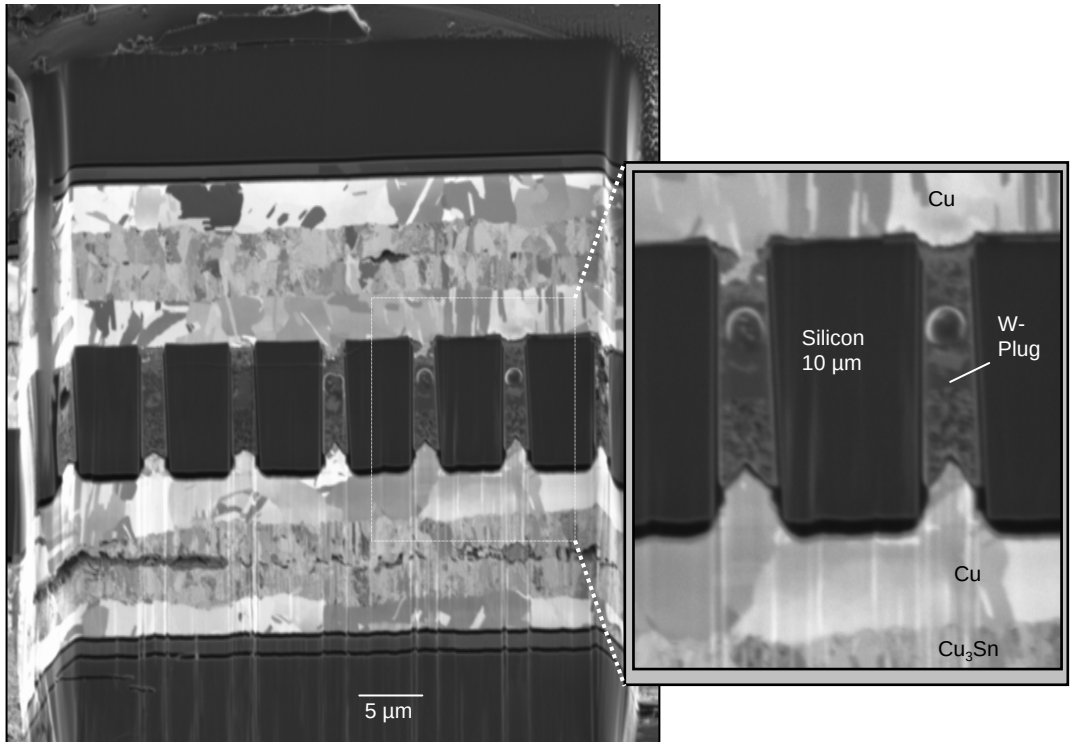
Top Chip; Layer 3

Soldering Layers

Pin Array of Medium Chip; Layer 2

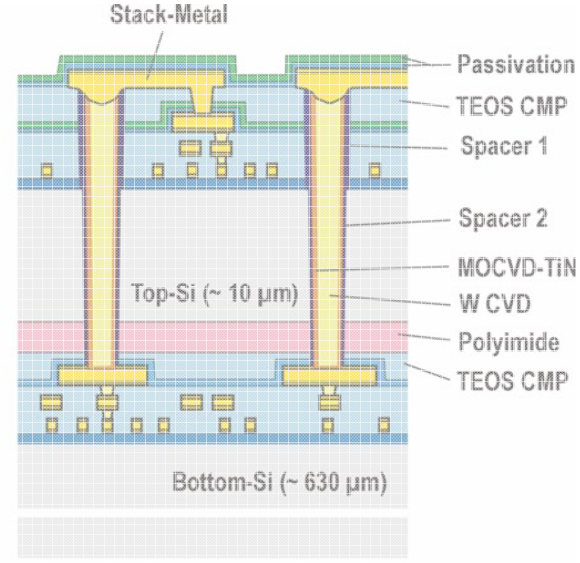
Soldering Layers

Bottom Chip; Layer 1



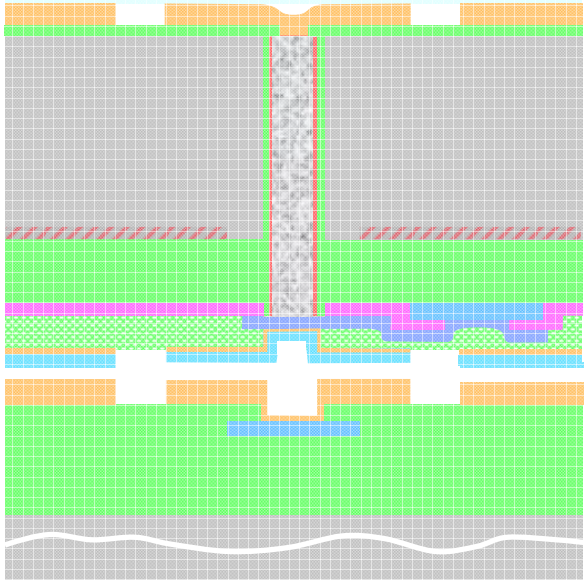
Vertical System Integration – *Three relevant Concepts (IZM-M)*

InterChip Via (ICV)



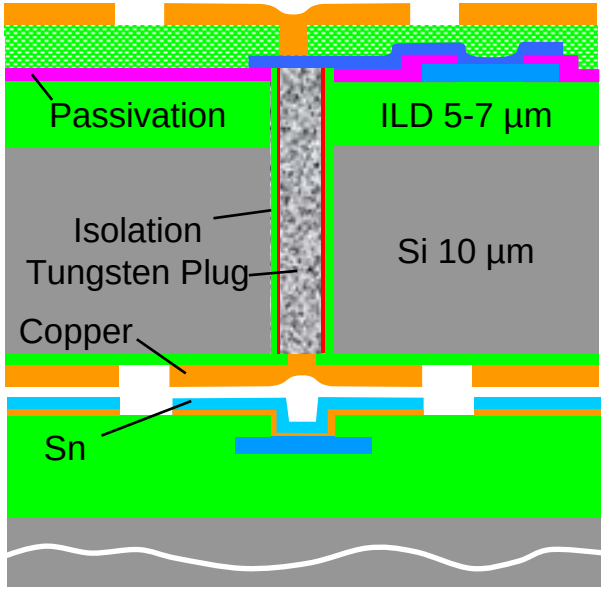
W-Plug / Polyimide

Face to Face modular (F2F-M)



W-Plug / Cu / Sn

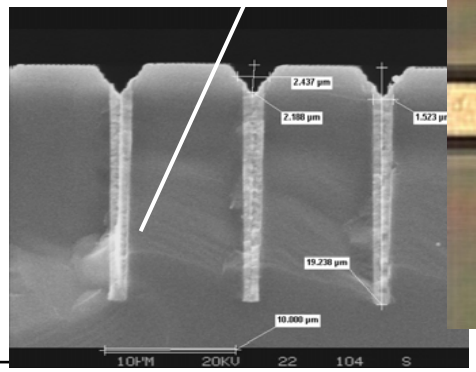
ICV / SLID

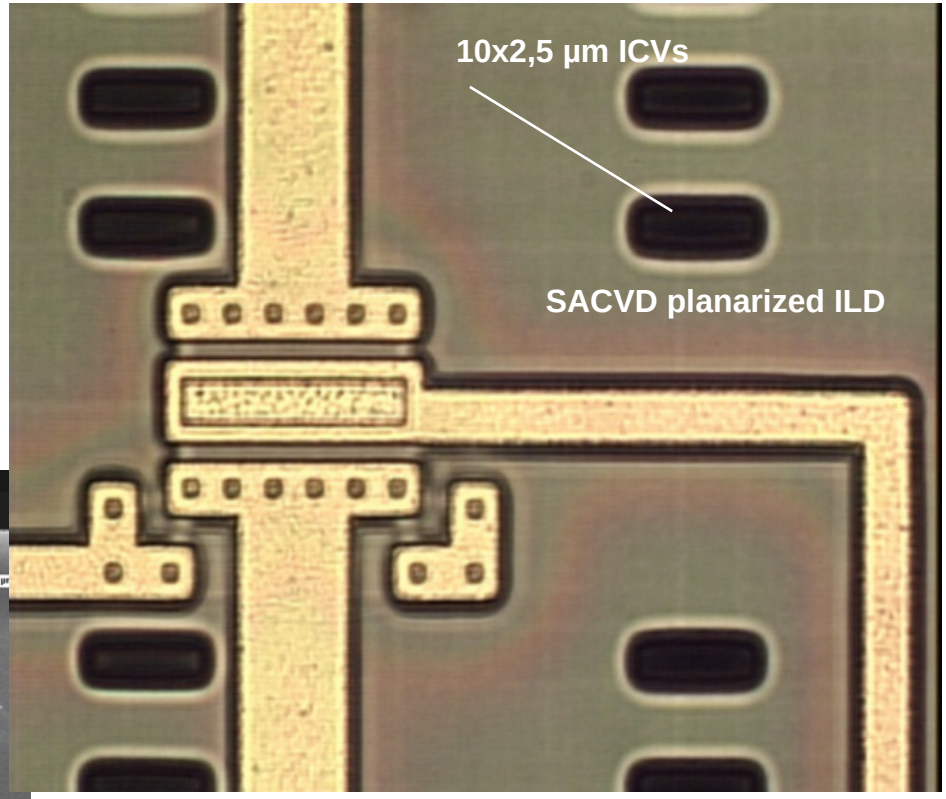


W-Plug / Cu / Sn

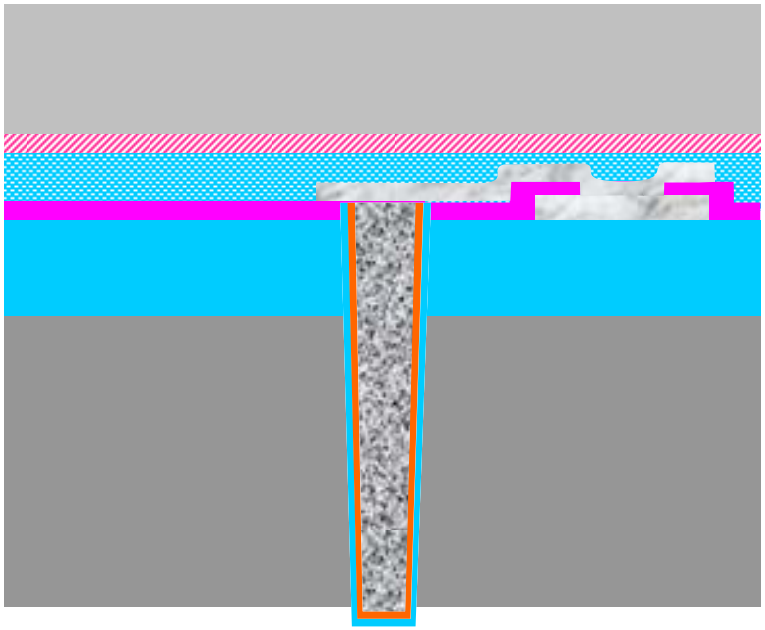
CMOS Top Wafer with ICVs after Trench Etching

- **Rectangular ICVs 10 x 2,5 µm, 20 µm deep, AR 8:1**
- **Distance between W-filled ICVs and Transistors:**
  ~ 4 µm to Source/Drain Area
  ~ 11 µm to Gate Area

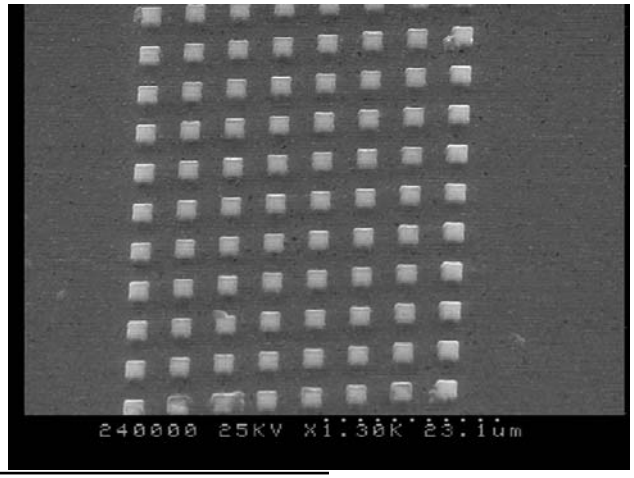




3D System Integration



- Fabrication of Tungsten-filled InterChip Vias on Top Substrate
- Via Opening and Metallization
- Bonding to Handling Substrate
- Thinning



Dr. A. Klumpp

Fraunhofer IZM
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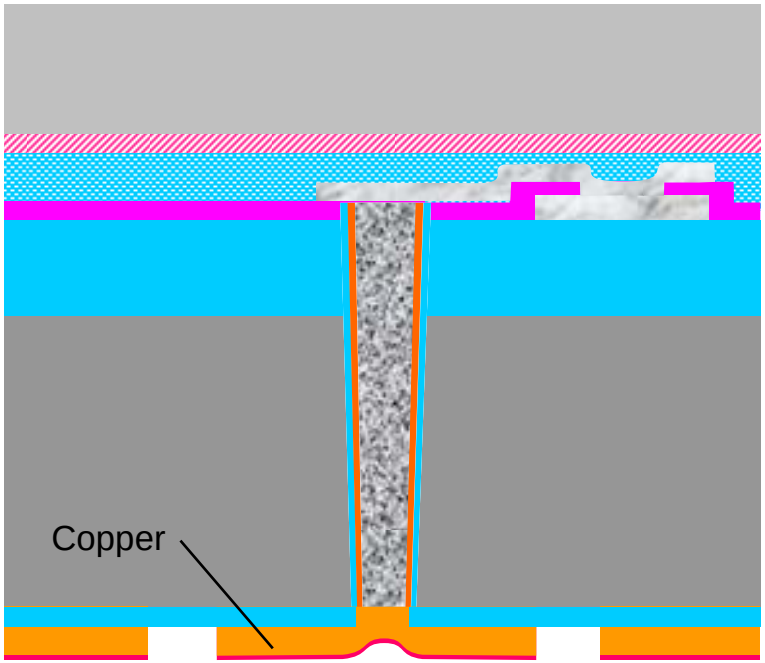
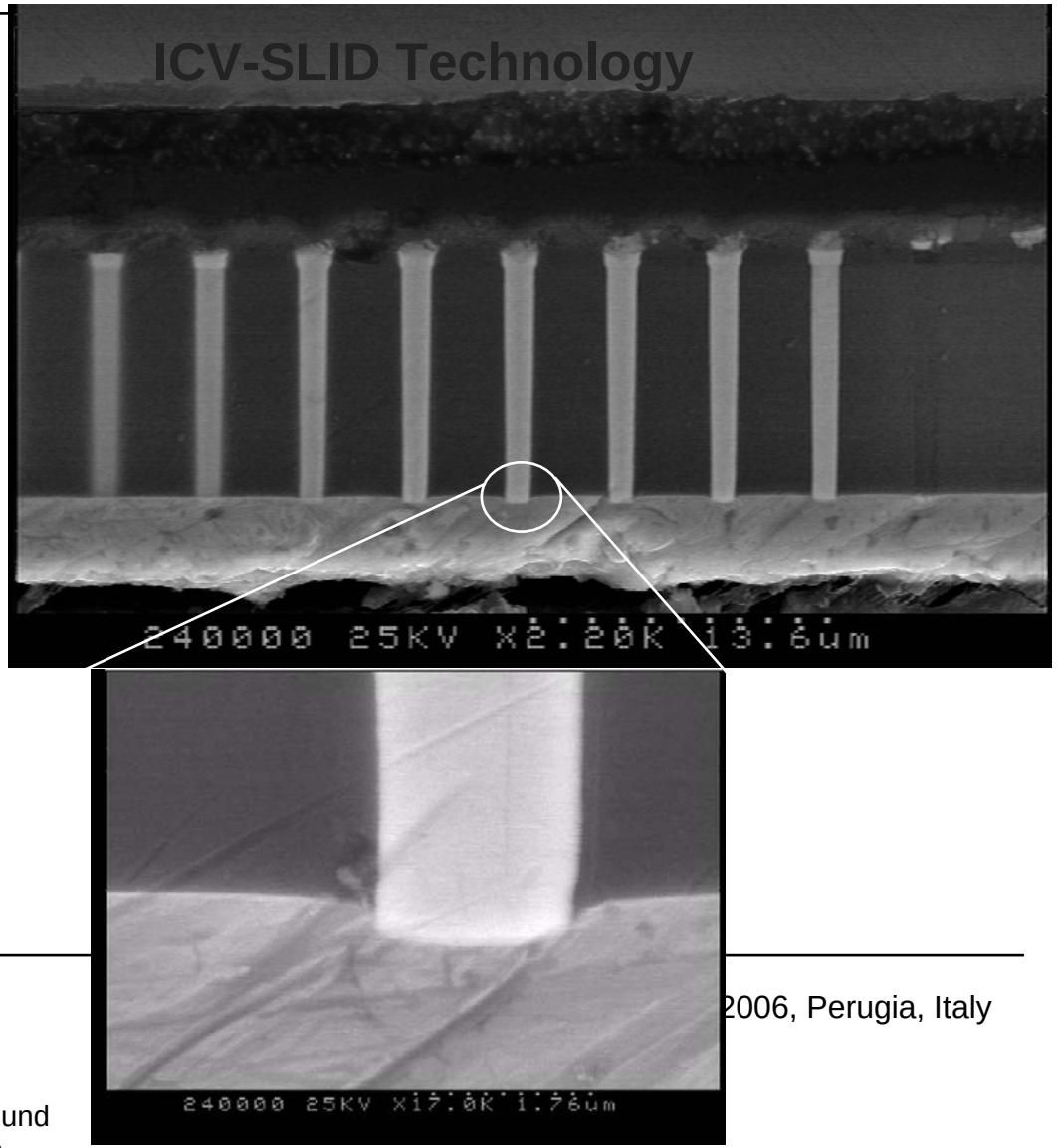
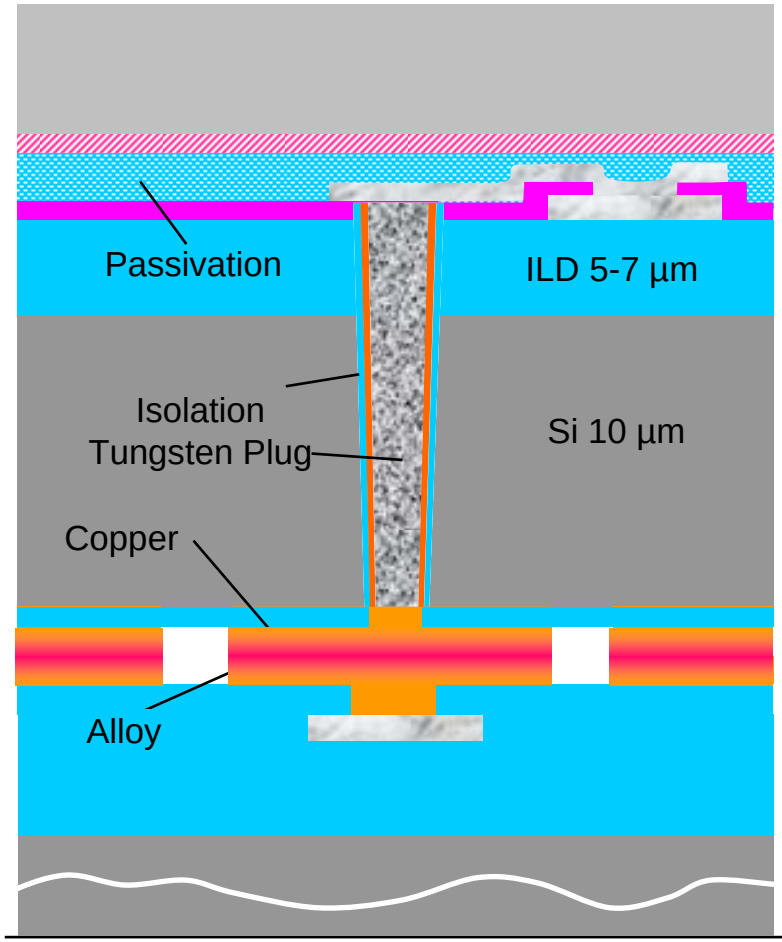
3D System Integration

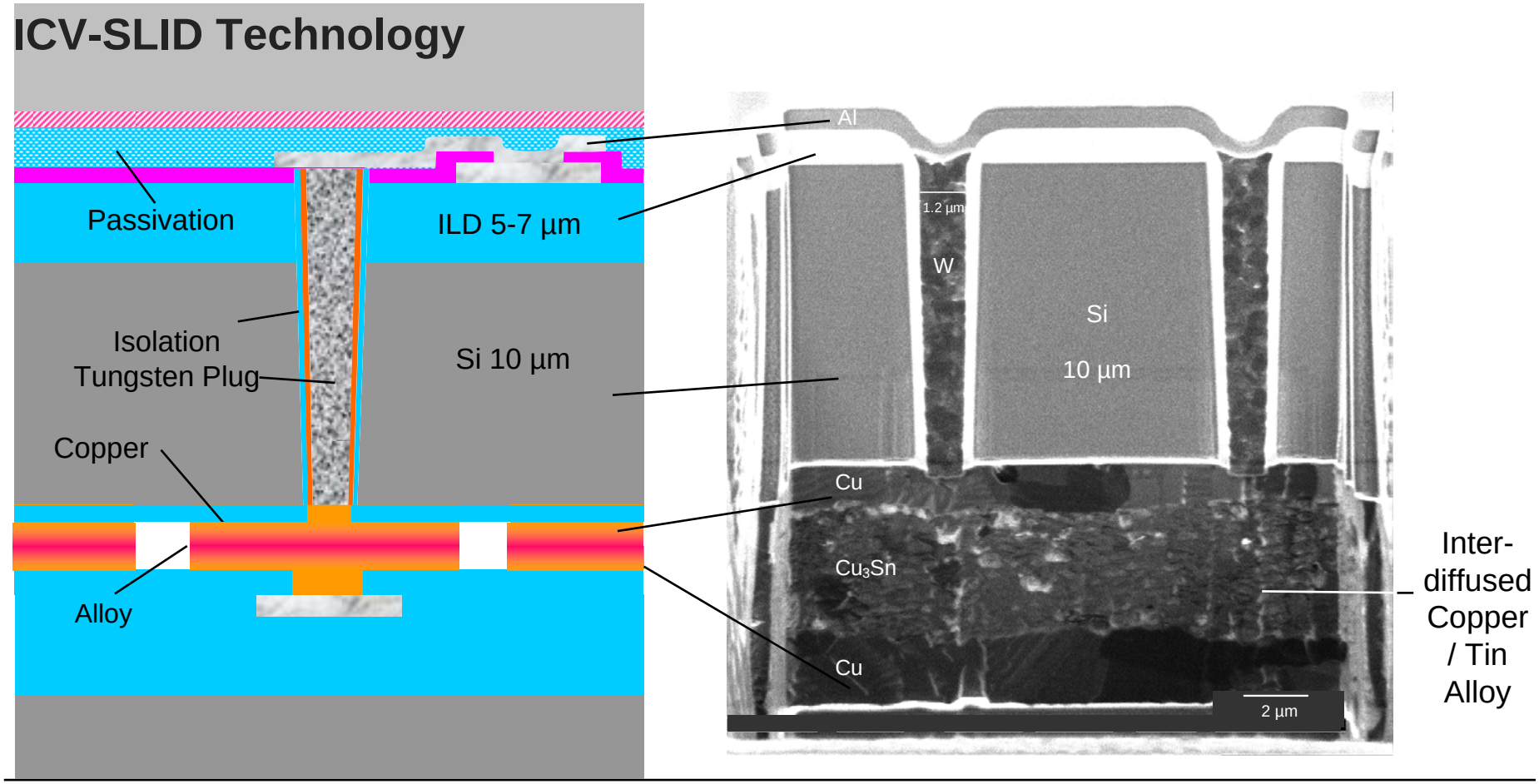






ICV-SLID Technology

- Fabrication of Tungsten-filled InterChip Vias on Top Substrate
- Via Opening and Metallization
- Thinning
- Opening of Plugs
- Through Mask Electroplating
- Alignment and Soldering



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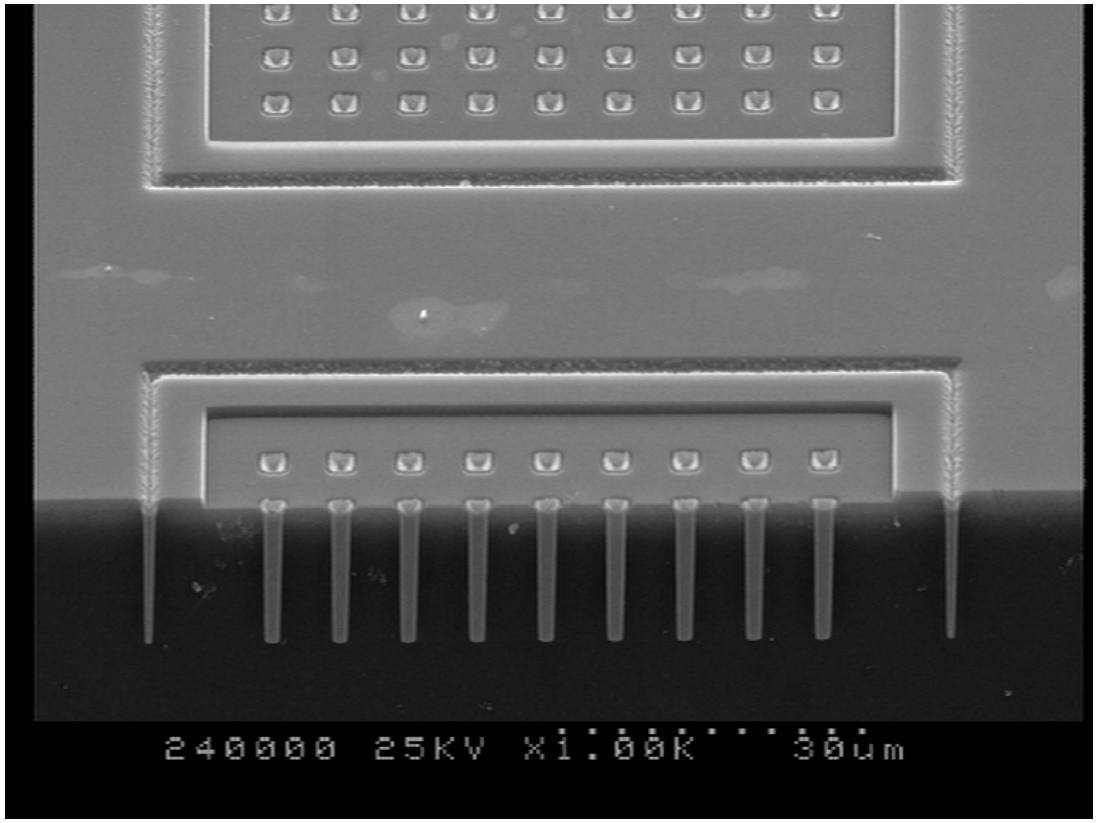
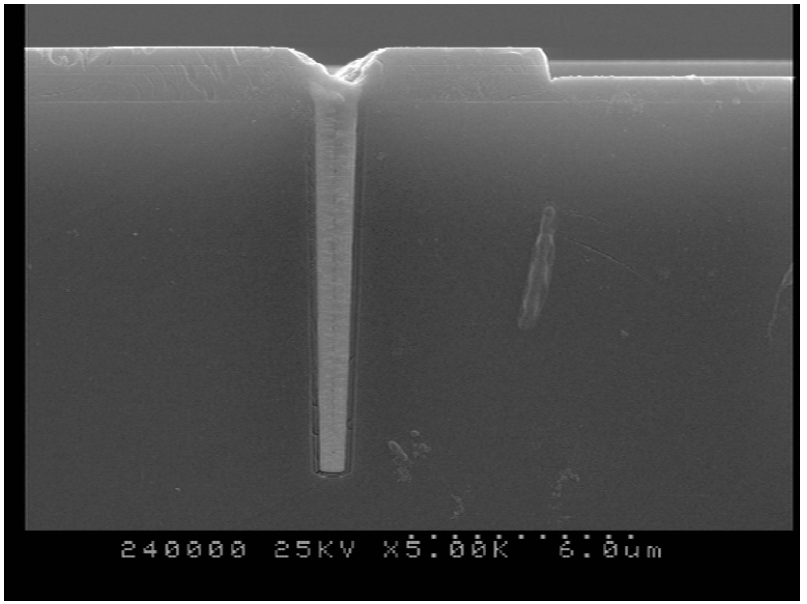
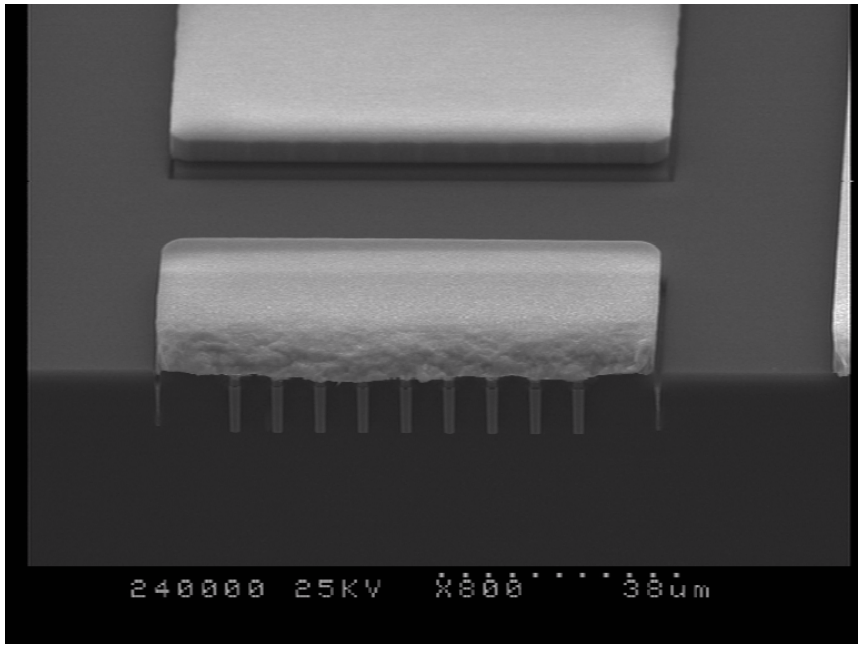
WL-CS-3D *- „low – Accuracy Placement“ Layout (1)*

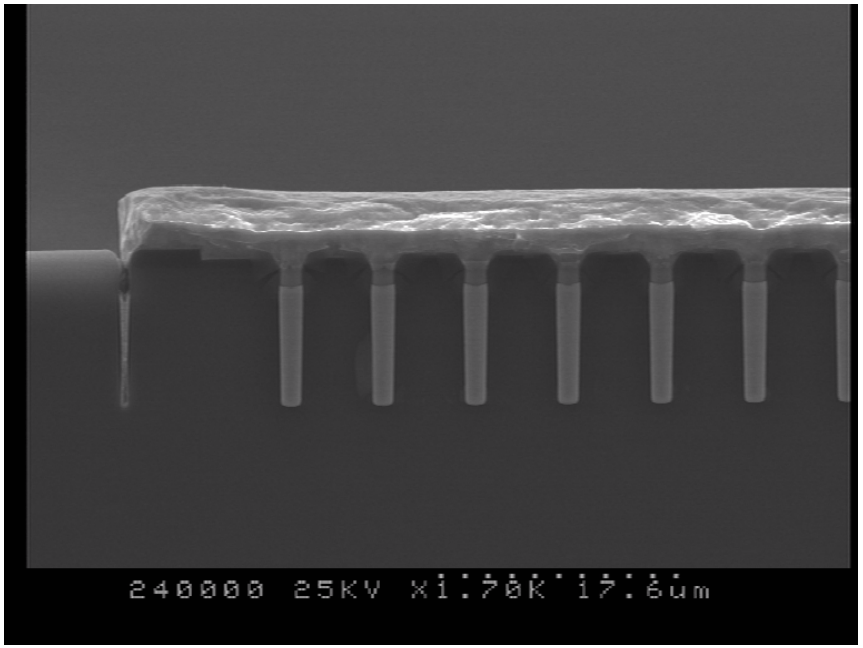


- Pin-Array and Isolation trenches
- combination of contact printing with stepper lithographie is possible



WL-CS-3D – *„low – Accuracy Placement“ Layout (2)*





- Copper pads on top of pin-array; development of „Electroplating prior to thinning“

Electrical Characterization

Electrical measurements

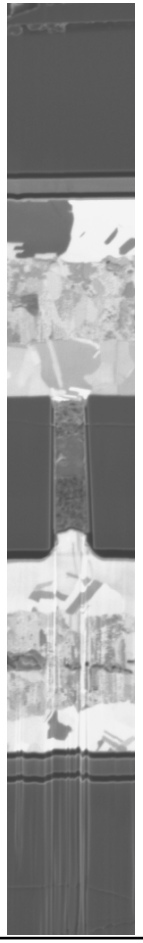
Measured values (from 240 element chain statistics):

Contact hole + soldering layers. ~0.43 Ohms

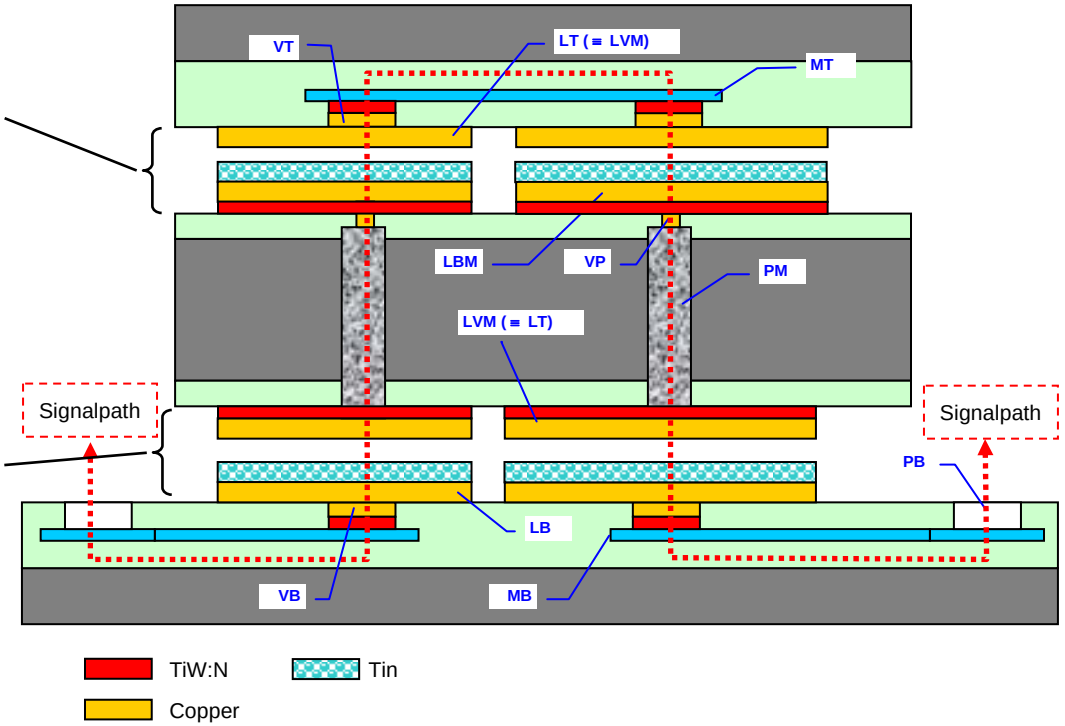
W-plug: ~ 1 Ohm

Contact hole + soldering layers. ~0.43 Ohms

Sum Value: 2.5 Ohm



Daisy Chains with up to 240 elements



Electrical measurements

- **Electrical Characterization on CMOS Wafers, prepared according to ICV-SLID Process Flow (without soldering transfer up to date)**
  - **No Evidence of significant Impact on MOS Transistors by 3D Process Sequence**
- **Interchip Via Characterization:**
  - **Good Electrical Isolation of ICVs to surrounding Silicon**
  - **Low resistance per Via:**
    - **1 Ohm, Pin only (2.5 x 2.5 µm2, 10 µm depth)**
    - **2.5 Ohm Via with SLID-Contacts**

Summary

Handling Concept

- Wafer-Level Chip-Scale Concept with Silicon Handling Substrate
- Simplified Handling of Thinned Silicon Wafers and Chips by Electrostatic Handling Substrate under Development

Integration Concepts

- Face-to-Face Modular / SLID with Flipped Device Orientation (die-down)
- Interchip Via and Interchip Via / SLID with Non-Flipped Orientation (die-up)

Concept Feasability

- Feasibility shown
- Applicability depends on Target Products and Cost of Ownership

Outlook (1)

- There still remain some keypoints to be worked out:
  - Thin Chip Handling (~10 µm) for Backside Processing (Batch or Single Chip)
  - Thermal Management (Simulation and Test Devices)
  - Compatibility to High Frequency Signal Transmission (70 ... x GHz)
  - Development of Very Low Cost Integration Sequences

Outlook (2)

- Further development of keypoints within two funded projects

  – KASS (*Communication and Automotive Applications in Stacked Silicon*)
  BMBF, Germany; 01.09.2005 – 31.08.2008; Status granted

  – e-Cubes
  European Community; 01.02.2006 – 31.01.2009;
  Status: Status granted

Thank you for your attention !