INTERCHIP VIA TECHNOLOGY BY USING COPPER FOR VERTICAL SYSTEM INTEGRATION

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ABSTRACT

The copper-based InterChip Via (ICV) technology was evaluated as a fully CMOS-compatible wafer-scale process for Vertical System Integration VSI®, that provides vertical electrical interchip interconnects placed at arbitrary locations, without intervention to the IC´s fabrication technologies. Key processes are the optically adjusted bonding of a thinned top wafer to a bottom wafer and the formation of copper-filled interchip vias through the thinned top wafer to the bottom wafer, providing a high-density vertical wiring between metallization levels of both wafers. The low temperature Cu deposition process provides excellent step coverage of nearly 100%. The high aspect ratio interchip vias could be filled completely and the developed total process sequence including MOCVD of TiN diffusion barrier and Cu/TiN etchback was used for the fabrication of vertically integrated wafer stacks. The electrical resistance of the Cu-filled interchip vias was characterized and compared to the results of the standard tungsten-based ICV technology.

INTRODUCTION

Vertical System Integration – the realization of 3-dimensional integrated systems by stacking and vertical interchip wiring of device substrates – is the key to significant advances in performance of microelectronic systems. This results from extensive parallelism, minimal interconnection length and elimination of speed limiting chip interconnects on a printed circuit board. Device layers, independently manufactured and tested, are vertically integrated into a 3D-chip (see Fig. 1). Thus for the potential user, VSI offers a maximum of flexibility to combine the advantages of different device technologies to realize systems-on-a-chip (SOC) instead of using expensive embedded technologies.

We developed the CMOS-compatible ICV technology that is based on the thinning and optically adjusted bonding of completely processed and electrically tested device substrates [1, 2]. The vertical interconnects are formed by fabrication of high aspect ratio interchip vias. The positioning of the ICVs is freely selectable. It was demonstrated that the yield and functionality of nonvolatile memory devices basically were not affected by the corresponding thinning and bonding processes [3]. The fully modular concept allows the formation of multiple device stacks.

The interchip vias are prepared on the top wafer by etching through all dielectric layers, followed by a typically 12 µm deep silicon trench etch. The top wafer is then adhesively bonded to a handling wafer and thinned with high uniformity until the trenches are opened from the rear. The bottom wafer is planarized and coated with polyimide, which serves as bonding layer. The stabilized top wafer and the primed bottom wafer are then optically adjusted and stacked. After bonding at approximately 400°C, the handling wafer is removed, leaving the desired wafer stack that can be further processed as a standard silicon wafer in a CMOS line. The interchip vias are opened to a metallization level of the bottom wafer. For lateral via isolation, a dielectric spacer technique is applied using highly conformal CVD of O_3/TEOS-oxide and the interchip vias are metallized by using MOCVD and etchback for metal plug formation. The lateral electrical connection of the metallized interchip vias to the metallization level of the top wafer is done by opening contact windows on the top wafer followed by a standard metallization.

The schematic cross section of a vertically integrated device stack is shown in Fig. 2. Finally, the bond pads are opened and the 3D-integrated devices can be tested, separated and mounted by use of standard procedures.

Initially tungsten CVD with a MOCVD TiN liner was used to fill the interchip vias with metal. The process and the electrical results of the ICV technology using W/TiN plugs for the vertical metallization are described elsewhere [3]. A yield and reliability test chip was designed and wafer stacks fabricated according to the ICV technology showed average contact resistances of 2.0 Ω for 2 x 2 µm² interchip vias and working contact chains with 10000 ICVs. The FIB cross section of a vertically integrated test structure in Fig. 3 shows a W-filled interchip via with its connections to the AlSiCu metallization of the top and the bottom device.

The reported results of the ICV technology by using tungsten are very promising [3]. However, in order to get the highest benefit from the vertical system integration, copper would be the desired material for the vertical metallization. This would not only show the potential to decrease the resistance of the interconnnect but also reduce the thermal budget of the process and the film stress in the interchip vias compared to the tungsten CVD approach. Easy integration with an on-chip copper metallization scheme of stacked high end chips will be a key advantage.

The first step is to replace the W plugs by Cu plugs and determine the feasibility and the electrical properties of this approach. Finally a full copper vertical interconnection is aimed at saving process steps by directly filling interchip vias and top metallization vias in one step and patterning the copper lines.

VERTICAL METALLIZATION OF HIGH ASPECT RATIO VIAS BY USING COPPER

The main focus of this chapter is the fill of the high aspect ratio (8 to 15) vias by copper CVD using MOCVD TiN diffusion barrier and the development of a Cu etchback process.

Experimental

For the experiments and development described hereafter, the interchip vias were etched into the top wafers and the spacer oxide with a thickness of 200 nm was deposited using a highly conformal ozone/TEOS PECVD process. Designed via diameters varied from 1.6 to 3.0 µm resulting in approximately 0.5 µm smaller actual vias to be filled (aspect ratio AR 8 to 15).

A PRECISION 5000 system (Applied Materials) was used for metal deposition (TiN + Cu). The system was equipped with two lamp heated tungsten chambers used for both Cu-CVD and TiN-CVD. The system runs with a wafer size of 150 mm. The wafers were kept in vacuum (about 30 mTorr) between TiN and Cu deposition.

TiN MOCVD using plasma densification

The metal organic precursor tetrakis-dimethylamino-titanium (TDMAT, ADCS, USA) was used for TiN deposition. The process consisted of subsequent cycles of the pyrolysis of TDMAT and a densification step by a N_2/H_2-plasma. 8 cycles were used to get a TiN thickness of 20 nm. The process in detail is described in [4]. For improving the adhesion of the MOCVD Cu at this TiN film an approximately 8 nm intermediate TiN film was deposited from the TDMAT precursor using a PECVD process.

Cu MOCVD

The metal organic precursor (hfac)Cu^{I}TMVS (CupraSelect®, Schumacher Corp., USA) was used for copper deposition. H(hfac)·$2H_2O$ (0.4 wt%) and TMVS (5 wt%) are mixed to the precursor as additives. The reaction mechanism and effect of the additives are described elsewhere [5]. The precursor was introduced into the chamber by a direct liquid delivery system.

The process conditions are listed in Table 1. For temperature and flow two values for an initial process and an optimised process are given.

Table 1: Process conditions Cu CVD

	Initial process	Optimised process
Temperature (Wafer)	ramp, 170°C...200°C	constant, 170°C
Precursor flow	600 mg/min...800mg/min, depending on temperature step	800 mg/min
Carrier gas flow	500 sccm Ar	
Chamber pressure	20 Torr	
Distance shower head – wafer	10 mm	

To improve the adhesion between Cu and TiN an in situ annealing step was performed initially at 450°C for 7 min in 50 Torr Ar atmosphere. To minimise the thermal budget, it has been shown that also 5 min annealing at 390°C is sufficient to get the same adhesion improvement. The investigations of different groups show the reason of the adhesion issues to be related to precursor chemistry (C and F interface contaminations) and at the same time to the surface state and reactivity of the diffusion barrier as base layer for the Cu MOCVD [6, 7]. The modified PECVD TiN barrier with increased Ti content provides either a more reactive surface forming Cu-Ti bonds at least during annealing or a surface which is less reactive with precursor or reaction byproducts minimising the interface contamination. Both effects lead to the observed improved adhesion and consequently high resolution XTEM revealed a distinct interface between Cu and TiN without any interfacial layer.

Cu etchback

Cu RIE in a Decoupled Plasma Source (DPS) chamber at a Centura mainframe (Applied Materials) using a chlorine based chemistry was applied to etch back the Cu and TiN barrier (ICP power 1.5 kW and bias power 0.5 kW). The wafers were heated up to approximately 300°C before metal etch using Ar sputtering. The etched wafers were processed without vacuum break in an ASP chamber using a hydrogen annealing at 375°C, 6 Torr for 20 min to avoid Cu corrosion.

Results

TiN MOCVD in high aspect ratio vias

The step coverage of the plasma densified CVD TiN was investigated by the deposition of an unusual thick TiN film of 84 nm (32 cycles of deposition and plasma treatment) and following cross-section SEM. As expected, the films showed an overconformal behaviour also in these extremely high aspect ratio features, but only in the upper part of the via. The lower thickness of films perpendicular to the wafer surface (field, via bottom) compared to the sidewall features is caused by the ion bombardment and the resulting higher densification at these locations. The results derived from about 1.1 and 2.0 µm wide vias, respectively, are summarised in Table 2. Even for the most aggressive aspect ratio of 15 the minimum film thickness is always above 33%. For the actual relevant via size with an aspect ratio of about 8 the bottom step coverage is 57%. The double film thickness at the via entrance compared to the sidewall near the bottom does not cause serious difficulties for the following Cu CVD fill as far as the TiN barrier thickness is kept at a thickness much smaller than the via diameter (20 nm).

Table 2: Step coverage of plasma treated MOCVD TiN in high aspect ratio interchip vias

Via size (design)	1.6 µm	2.5 µm
Via size (measured)	1.1 µm	2.0 µm
Aspect Ratio	~ 15	~ 8
Field top	81 nm = 100%	81 nm = 100%
via entrance	110 nm = 136%	103 nm = 127%
sidewall middle	59 nm = 73%	63 nm = 78 %
via bottom	27 nm = 33%	46 nm = 57%

MOCVD Cu fill of interchip vias

CVD is able to provide excellent step coverage when operating in the reaction rate limited regime, where always a sufficient amount of precursor is delivered to the surface. At a given maximum precursor flow, this regime is achieved by applying low temperatures. For our given parameters at the system this is achieved at a wafer temperature of about 200°C and below for 800 mg/min precursor flow (see Fig. 4). Depositions at 170°C and 200°C have been carried out at interchip vias to prove this behaviour also with respect to step coverage. The minimum step coverage was observed at the via bottom. Only for the low temperature process at 170°C a perfectly 100% step coverage was observed at the via sidewalls, whereas depositions at 200°C show a step coverage of 65%. Unfortunately, the deposition rate is low for the low temperature process. Therefore, the initial process to completely fill the interchip vias used a temperature ramp from 170°C to 200°C shown in Fig. 5. This process was optimized to fill features with an aspect ratio of 4 at via diameters down to 0.25 µm with a high deposition rate. Applying this process to interchip vias of AR 8.5 the minimum step coverage was determined to be 80% after 500 s of total process time (resulting film thickness on top: approx. 400 nm). Further via fill leads to incomplete fill of the plug (Fig. 6).

The very high aspect ratio therefore calls for the 100% step coverage which was achieved using a constant temperature of 170°C. Fig. 7 shows that with this process the via could be filled completely. Only some small voids are left after annealing.

Cu etchback process for Cu plug formation

Fig. 8 demonstrates that the chlorine based RIE etchback process provides a clean surface of the passivation. A plasma emission endpoint detection system was used to detect the etch stop. The etch selectivity of the Cu to the underlying CVD TEOS Oxide is about 2:1.

PROCESS INTEGRATION

To evaluate the electrically features of the copper-filled interchip vias, stacked wafers of the yield and reliability test chip were processed. The interchip vias were filled with the developed technology by TiN MOCVD, Cu MOCVD and Cu etchback. To provide a good interface between the Cu plug and the bottom wafer AlSiCu metallization, different cleaning steps were investigated. An applied wet cleaning with EKC 265 solution led to a lateral attack of the polyimide / Si interface in the interchip via which can not be tolerated. Argon sputter etch was evaluated at tungsten filled plugs resulting in no change of the measured via resistance. It is assumed, that in such high aspect ratio structures the effectiveness of the sputter etch clean at the via bottom is very restricted. For Cu/TiN/Cu metallization it could be shown, that a sufficiently low via resistance can be achieved even without cleaning. The specific contact resistance measured between metal 1 and metal 2 both TiN/Cu/WN (bottom/top) by etching the via down through the top WN barrier to the metal 1 Cu was always below 1.6 Ωµm² (Fig. 9). Therefore, also

Cu/TiN/AlSiCu interchip via structures were prepared initially without an appropriate via clean. An AlSiCu metallization was used to connect the filled interchip vias to the top wafer metallization. The FIB cross section of a such prepared test structure is shown in Fig. 10. Although no interfacial layer is visible in the FIB cross section, the derived specific via resistance was measured to be about 3 times higher compared to W filled interchip vias (10.8 Ωμm² for Cu ICV versus 3.6 Ωμm² for W ICV). FIB preparation and following measurements at Cu vias with different heights show via resistances independent on the via geometry. This indicates an interface contamination at the lower via interface (bottom wafer Al and TiN/Cu interchip via). This behavior is attributed to a longer storage time before via fill for the Cu ICVs compared to the W ICVs which causes an oxidation of the Al surface in the open via. Consequently, particularly for the Cu/TiN/AlSiCu interface an appropriate cleaning process has to be developed, which is preferably a compatible wet cleaning step.

CONCLUSIONS

A fully CMOS-compatible wafer-scale process for Vertical System Integration VSI® was evaluated. The vertical interconnects were realized by copper-filled interchip vias. In a first approach, the feasibility and the electrical properties of the copper-based ICV technology were determined by using Cu-filled interchip vias lateral connected by standard Al metallization to the metal level of the top device. Deposition and etching were carried out on standard industrial equipment and are fully compatible to microelectronic back end of line. Copper CVD and copper RIE are not mainstream processes, but they are much more suitable for this application than mainstream processes are. The large absolute depth (15 μm) makes electroplating of copper very complicated. The etchback process induces a much lower mechanical stress to the stacked wafers than a CMP process. Furthermore, the VSI process flow makes Cu damascene technology particularly the trench etch while having opened interchip vias more complex compared to a Cu RIE approach.

Wafer stacks fabricated according to the VSI process sequence showed completely filled Cu interchip vias. However, the evaluated Cu-based ICV technology did not result in an improvement of the ICV contact resistance in comparison with the W-based technology as reference. This effect was obviously caused by a contamination problem at the lower interface of the Cu plug, between the TiN barrier and the Al metallization. It could be shown that in the case of vertically integrated devices with Cu metallization the specific contact resistance can be as low as 1.6 Ωμm² for the relevant contact scheme Cu/TiN/Cu.

As promising result for the future fabrication of multilayered 3-dimensional integrated systems, the process integration of the copper metallization into the interchip via technology could be successfully demonstrated, showing the potential of cost reduction for vertical system integration.

REFERENCES

[1] P. Ramm et al., Microelectronic Engineering 37/38, 39-47 (1997).
[2] P. Ramm, R. Buchner, “Method of making a three-dimensional integrated circuit”, U.S. Patent No. 5,563,084 (8 October 1996)
[3] P. Ramm et al., Proc. International Interconnect Technology Conference IITC 2001, 160-162
[4] S. Riedel, S.E. Schulz, T. Gessner, Microelectronic Engineering 50, 533-540 (2000).
[5] J. Röber, S. Riedel, S.E. Schulz, T. Gessner, Microelectronic Engineering 37/38, 111-119 (1997).
[6] S. Riedel, K. Weiss, S.E. Schulz, T. Gessner, Advanced Metallization Conference in 1999, Orlando, Mater. Res. Soc. Conf. Proc. AMC 1999, Warrendale, PA, 195 (2000)
[7] V.M. Donnelly, M.E. Gross, J. Vac. Sci. Technol. A11, 66 (1993)

ILLUSTRATIONS

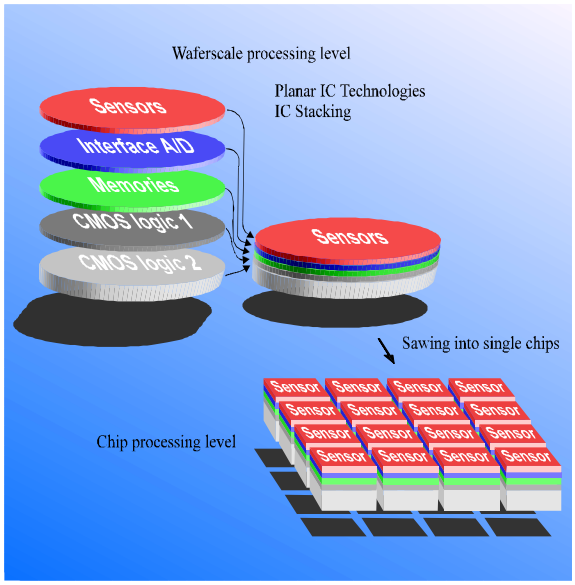

Fig. 1: Vertical System Integration VSI®

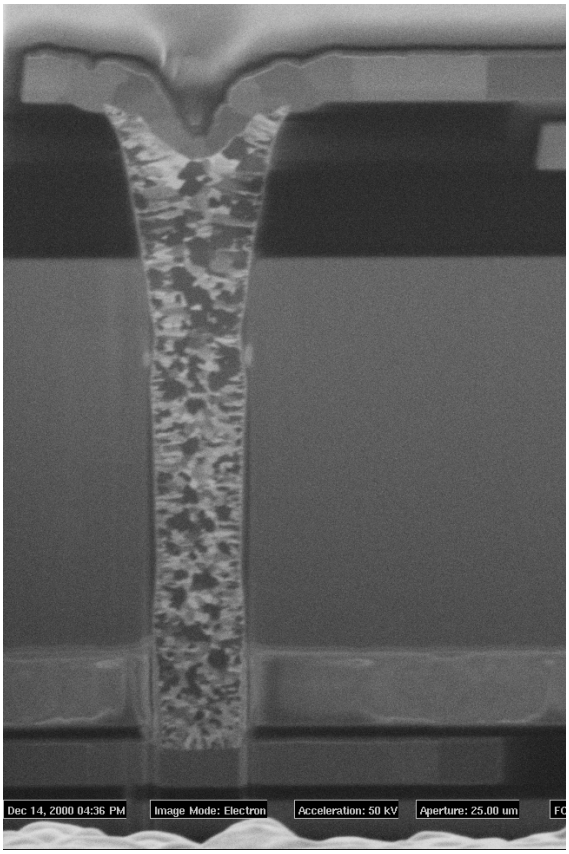

Fig. 3: Vertically integrated test chip structure showing a 2.5 x 2.5 µm² W-filled interchip via

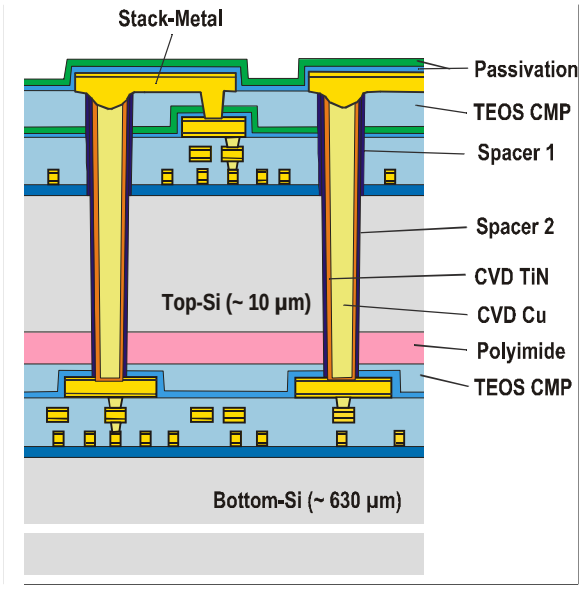

Fig. 2: InterChipVia technology (ICV) – schematic of a vertically integrated device stack

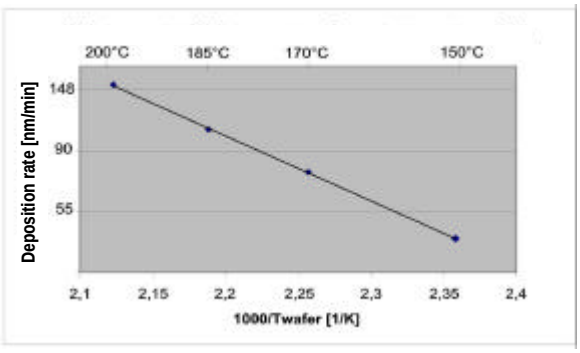

Fig. 4: Arrhenius plot of the Cu deposition rate at 800 mg/min CupraSelect flow and process conditions given in table 1

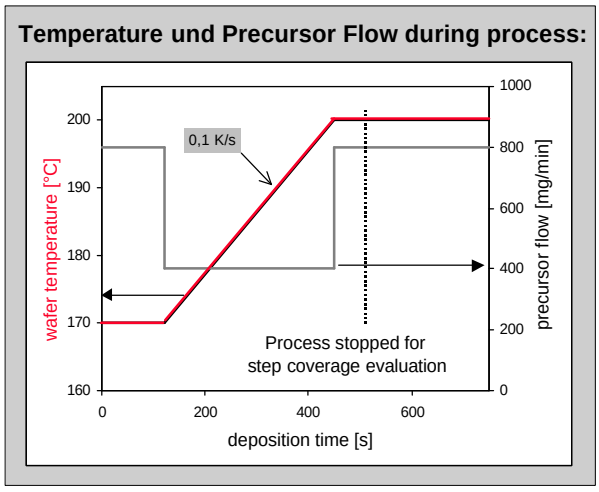

Fig. 5: Designed temperature ramp Cu CVD process for optimal deposition rate and step coverage at the same time

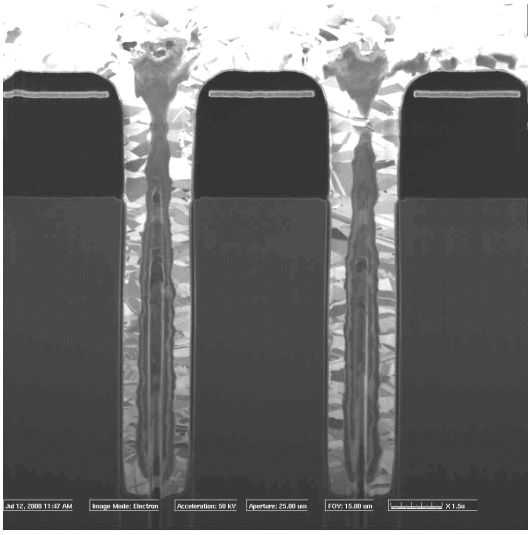

Fig. 6: Incompletely filled 3.0 x 3.0 µm² vias using a temperature ramp (170°…200°C) copper CVD process showing overhangs (FIB)

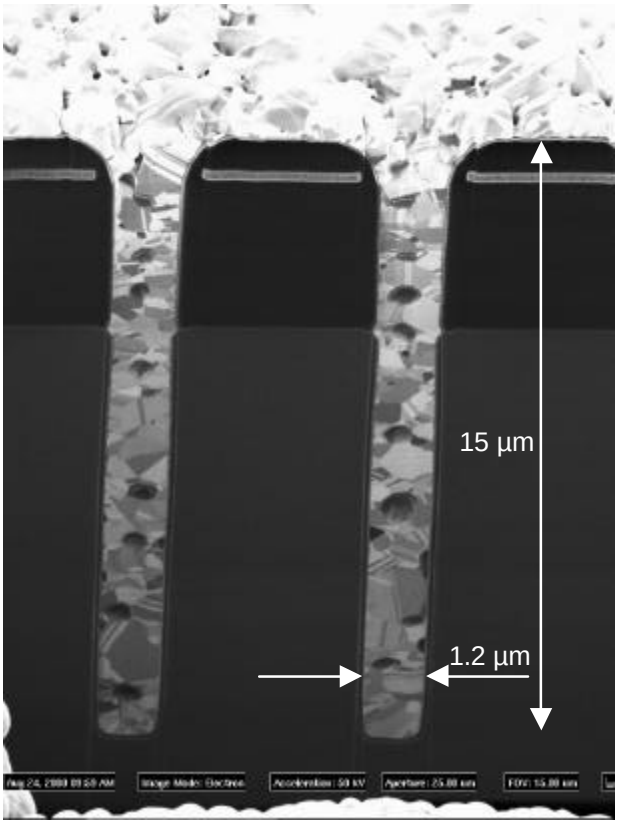

Fig. 7: Copper-filled vias with AR 12.5 after Cu CVD at 170°C and anneal (FIB)

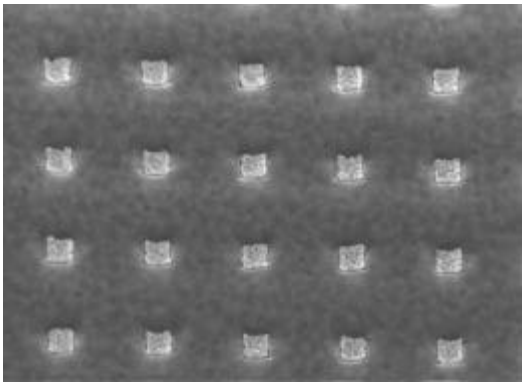

Fig. 8: Residue free etchback of the Cu/TiN-bilayer for copper plug formation (SEM)

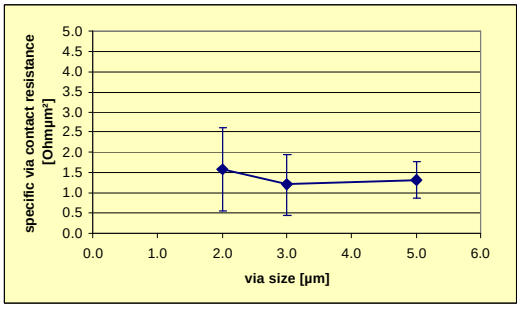

Fig. 9: Cu/Cu via resistance (Kelvin method)

Fig. 10: FIB cut of a vertically integrated test chip structure, showing a 2.5 x 2.5 µm² copper-filled interchip via with its connections to the Al metal levels of the top and the bottom device