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ATLAS High Luminosity Tracker Upgrade Workshop, Liverpool, 6-8 Dec 2006

R&D for a novel pixel detector for SLHC

MPI Munich SLHC Upgrade Group

L. Andricek, J. Dubbert, N. Ghodbane, O. Kortner, H. Kroha, H.-G. Moser, R. Nisius, R. Richter

Novel pixel detector concept based on thin FZ detectors and 3D interconnection technology

(R&D proposal in preparation)

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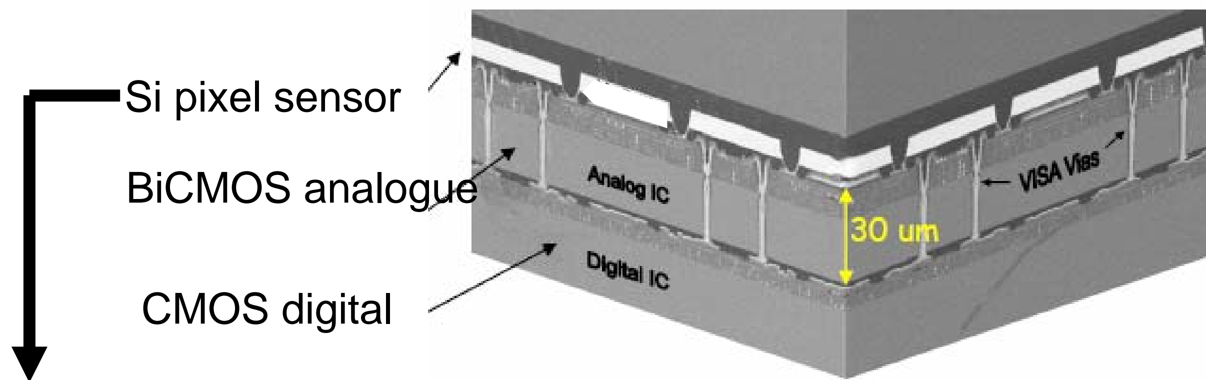
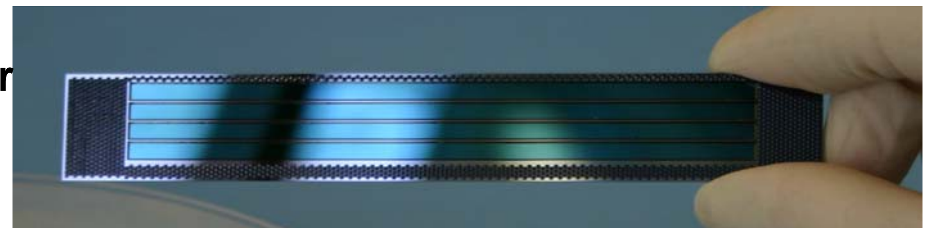
R&D for a novel pixel detector for SLHC

3D interconnection (sensor – electronics; electronics – electronics):

Alternative to bump bonding (fine pitch, potentially low cost?).
New possibilities for ASIC architecture (multilayer, size reduction).
Optimization of rad. hardness, speed, power.
Impact on module design (ultra thin ASICs, top contact, 4-side buttable).



R&D on thin (O(50μm) FZ silicon detectors:
Based on well known pixel sensor technology.
Can be operated at 10^{16} n/cm^2 (V_{dep}, I_{leak}, CCE).



Can lead to an advanced module design: rad hard with low material budget

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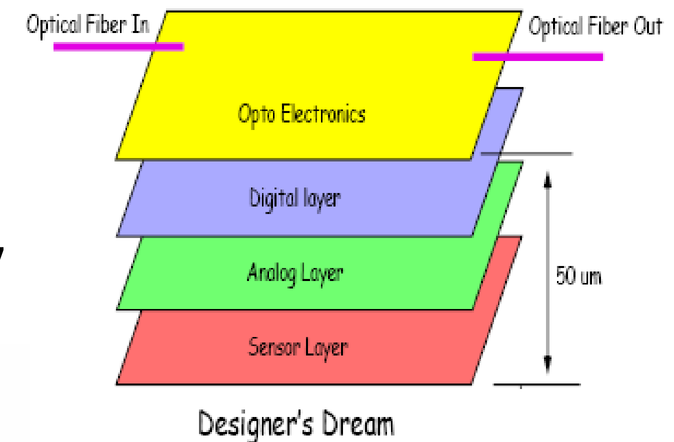
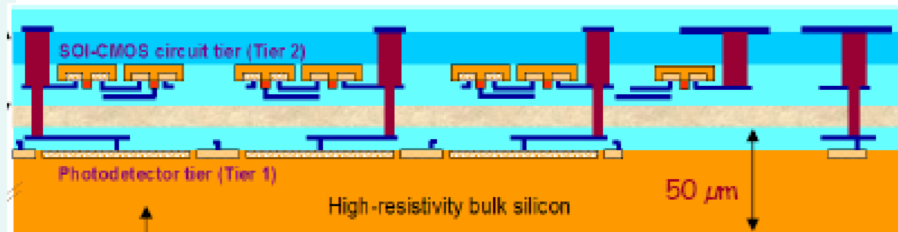
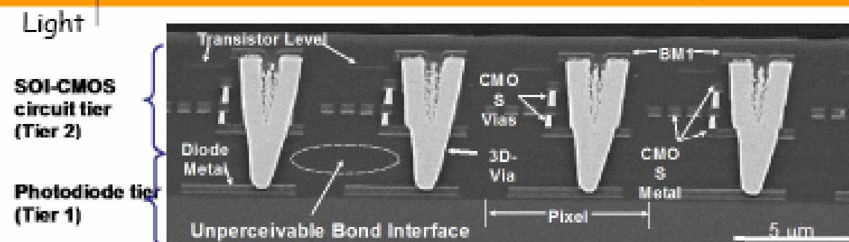
3D Interconnection

2 or more layers (="tiers") of thinned semiconductor devices interconnected to form a "monolithic" circuit.

- **Different layers can be made in different technology (BiCMOS, deep sub-µ CMOS, SiGe,…..).**
- **3D is driven by industry:**
  - **Reduces R,L and C.**
  - **Improves speed.**
  - **Reduces interconnect power, x-talk.**
  - **Reduces chip size.**
  - **Each layer can be optimized individually**







Drawing and SEM Cross section

For HEP: sensor layer: fully depleted Si
Example: 2-Tier CMOS Sensor, 1024 x 1024 pixel, pitch 8 µm by MIT-Lincoln Lab

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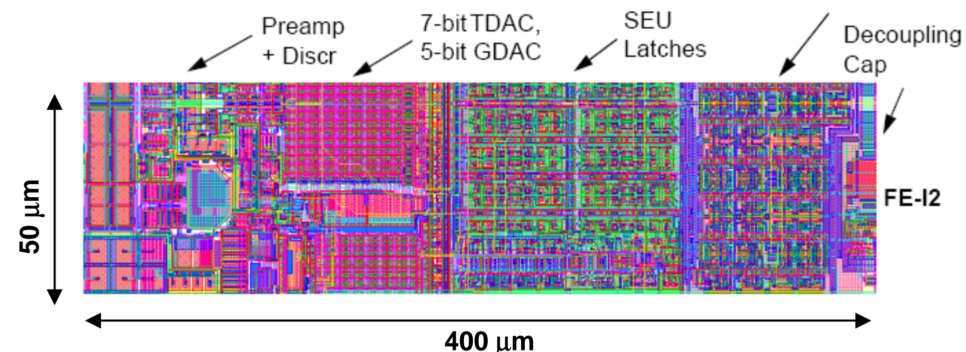
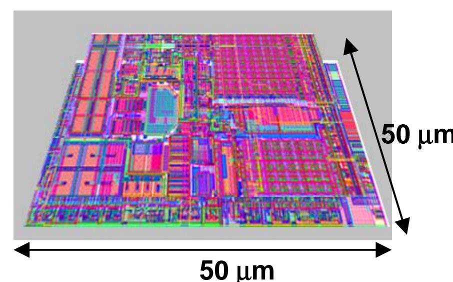
Advantages of 3D

Multilayer electronics:

Split analogue and digital part
Use different, individually optimized technologies:

-> gain in performance, power, speed, rad-hardness, complexity.
-> smaller area (reduce pixel size or add functionality).



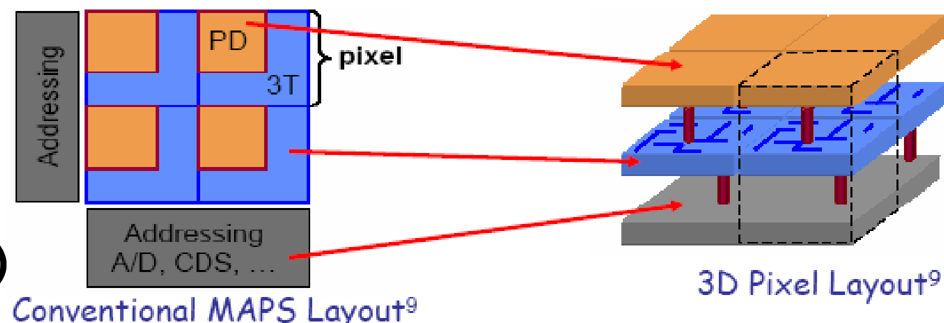


50 x 400 μm^2 (0.25 μm)
May shrink to ~ 50 x 50 μm^2 (130 nm)

4-side buttable devices:

-> no dead space.
-> simpler module layout.
-> larger modules.

(reduce complexity and material)



Conventional MAPS Layout[9]

3D Pixel Layout[9]

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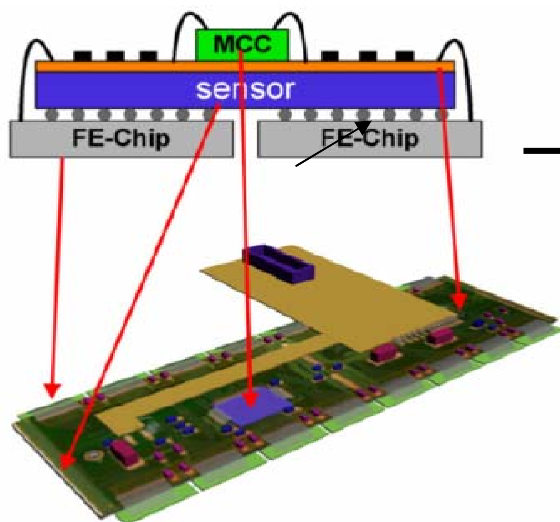
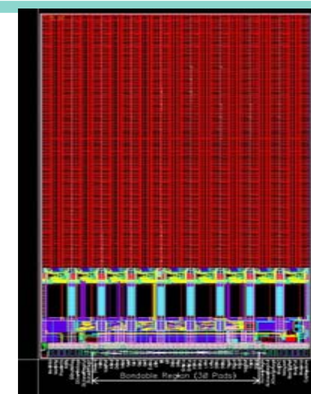
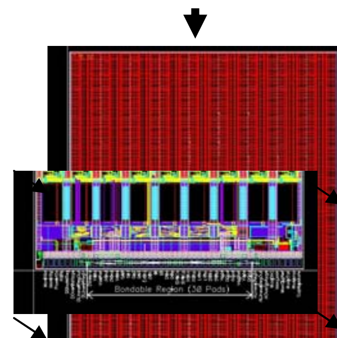
Advantages for Module Design

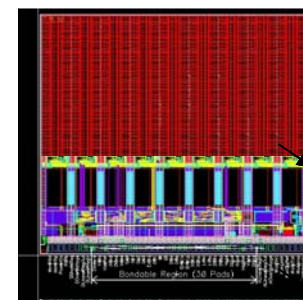


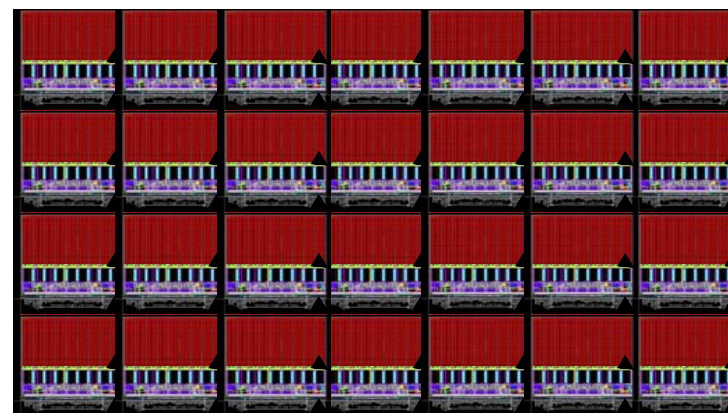


Pixel area (facing sensor)

Pipeline and control
Bond pads (cantilever)







Control on top of pixel area.
External contact from top.
Contact pixels through vias:
-> 4-side buttable.
-> No “cantilever” needed.

Larger module with minimal dead space.

Less support structures & services.
Substantial material savings.

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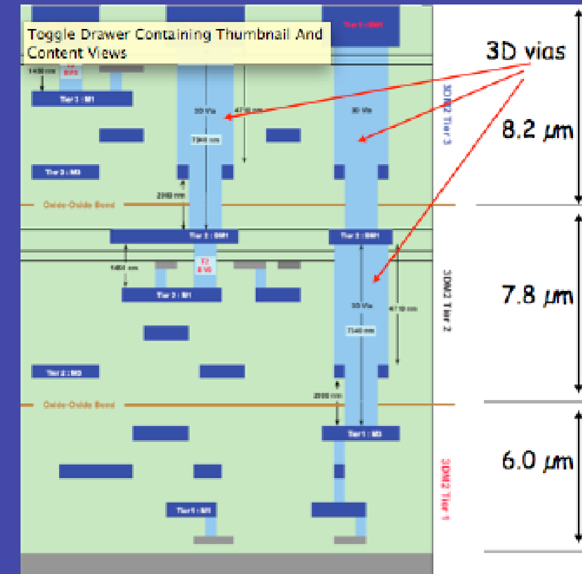
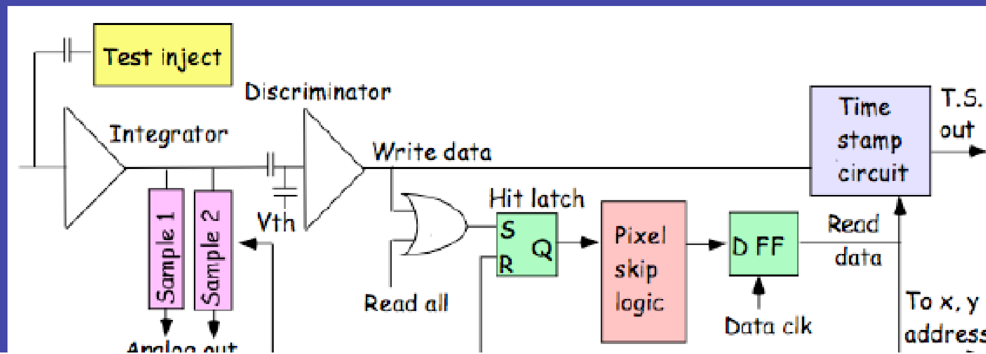
3D R&D at Fermilab

3D ILC Chip

- Fermilab has contributed an ILC readout chip design to a MIT-LL 0.18 micron three tier SOI 3D multiproject run
- ~2.5 mm x 2.5 mm chip, 64x64 20 micron pixels
- Does not include sensor integration
  - Bond readout circuit to an independent sensor wafer (precursor to full 3D integration run)
- Design includes amp/disc, time stamp, pixel control, token passing -





–Store analog and digital time stamps in the hit pixel cell.
–Store double correlated sample in pixel

R. Lipton (Fermilab): submitted to MIT-LL

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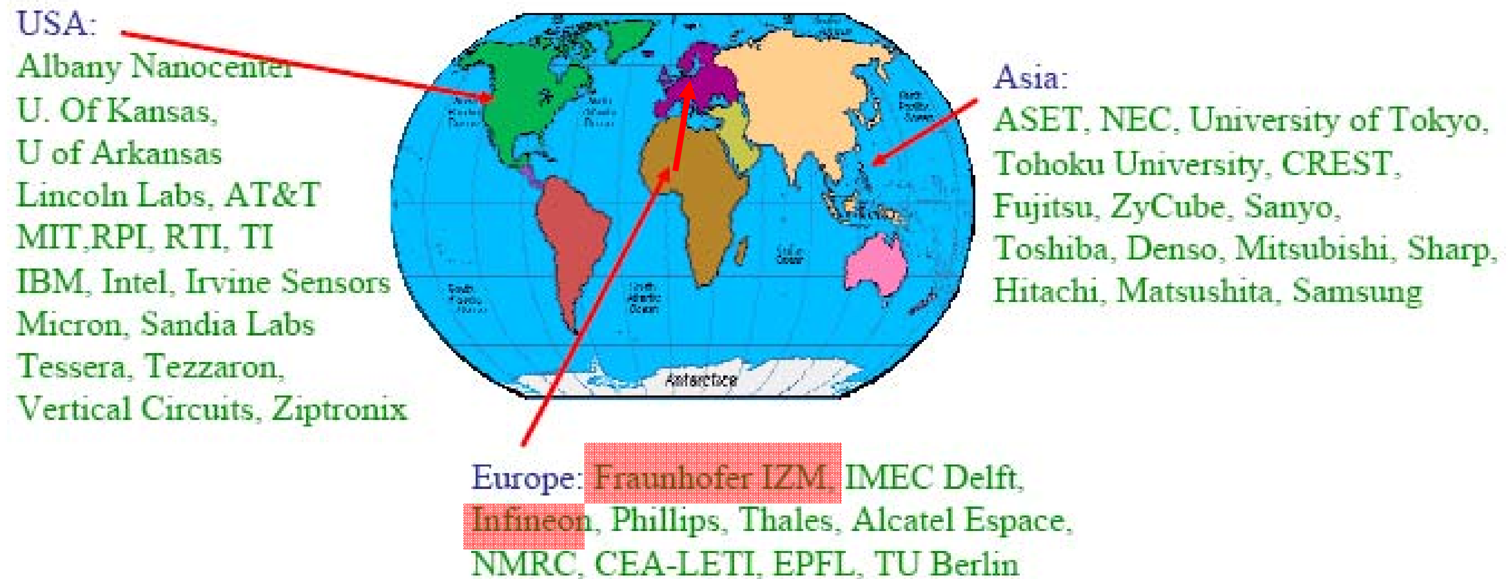
World Wide Interest in 3D



R. Yarema (Fermilab)

3D is discussed in the ITRS (International Technology Roadmap for Semiconductors) as an approach to improve circuit performance and permit continuation of Moore's Law.

R&D driven by industry.
Different approaches (solder, SOI, epoxy).

MPI will work with Fraunhofer IZM, Munich.

IZM SLID Process

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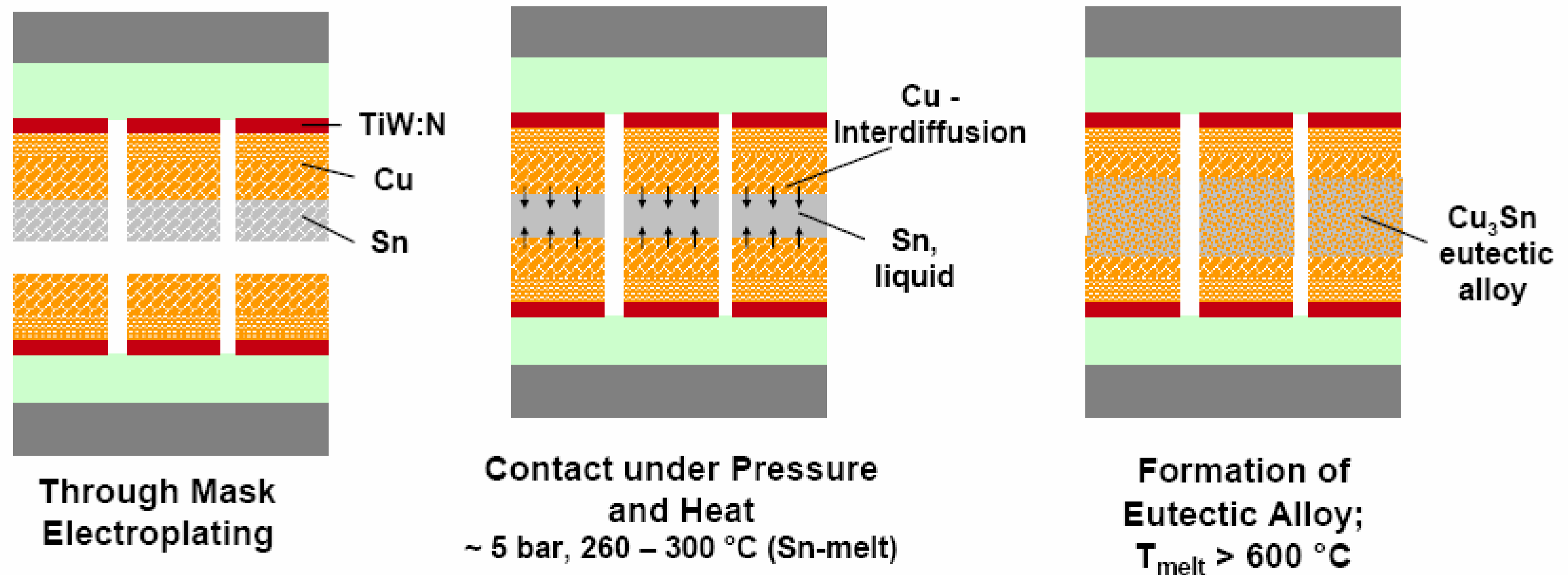
Metallization SLID (Solid Liquid Interdiffusion)



- Alternative to bump bonding (less process steps “low cost” (IZM)).
- Small pitch possible (< 20 μm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

Fraunhofer IZM Institut Zuverlässigkeit und Mikrointegration

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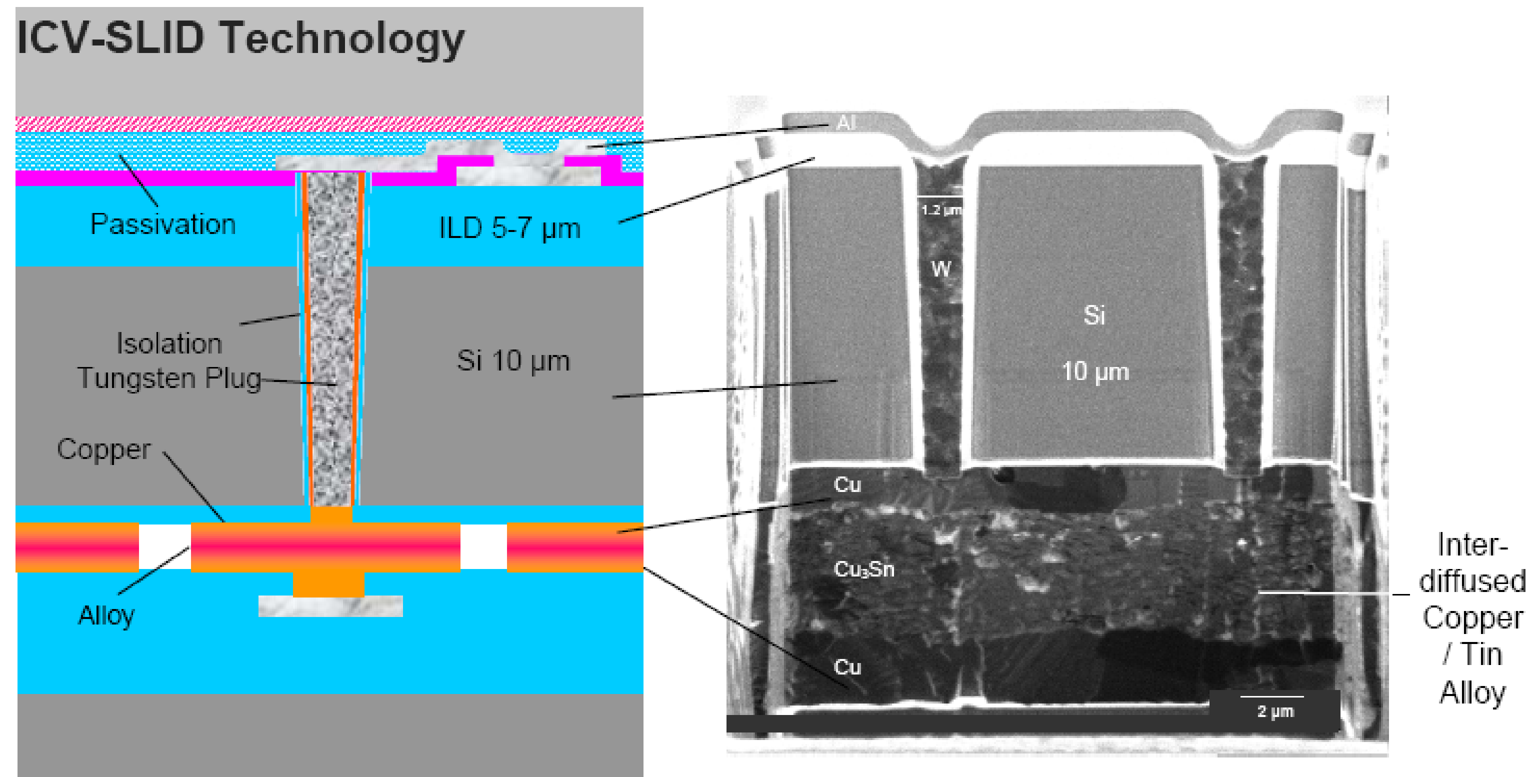
Through Silicon Vias



ICV = Inter Chip Vias

Fraunhofer IZM Institut Zuverlässigkeit und Mikrointegration

- Hole etching and chip thinning
- Via formation with W-plugs.
- Face to face or die up connections.
- 2.5 Ohm/per via (including SLID).
- No significant impact on chip performance (MOS transistors).

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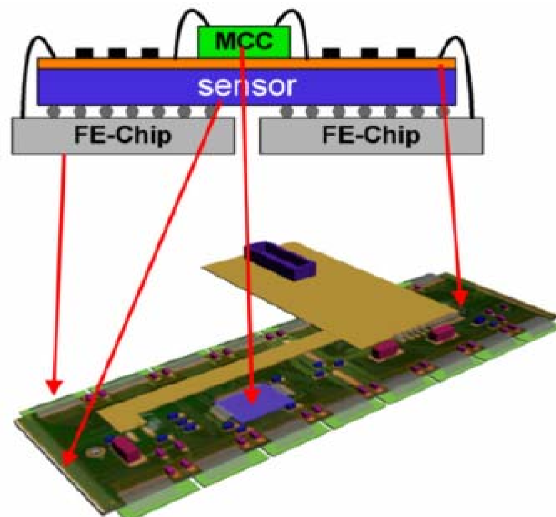
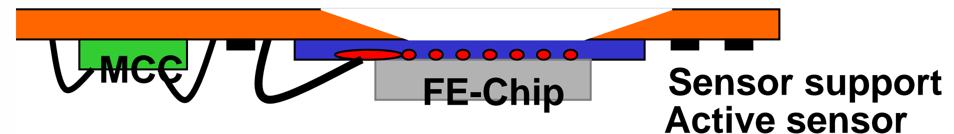
R&D Program

a) Test interconnection process with diode test structures:
- Post processing of test wafers (barriers, electroplating..).
- Test leakage currents, interconnection R and C, yield.

b) Build demonstrator using ATLAS pixel chip and pixel sensors made by MPI:
- Unthinned ASICs, no vias.
- With thinning of pixel chip & vias.

c) In parallel: Module and ASIC concepts making use of 3D possibilities.





As pixel sensor: use thin FZ sensors made at MPI:
- Available.
- Important R&D by its own!

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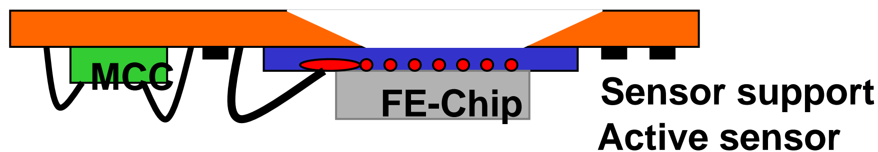
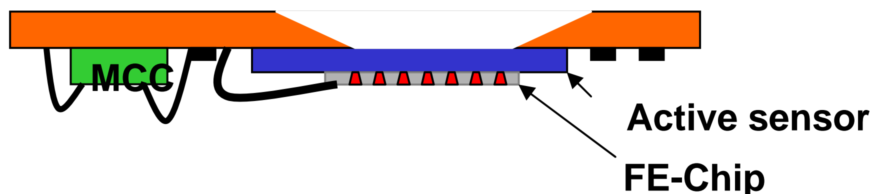
Alternatives

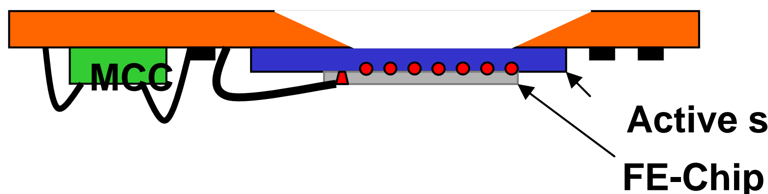


a) **Simple connection of FE chip face to face "Fan-out" on for service connections (using Cu-layers on sensor). No thinning of AISC needed.**



b) **Thinned FE chip with etched vias to sensor. Standard bondpads for services are accessible.**

(impossible to etch vias to bump bond pads of ATLAS chip ?)



c) **Connect FE-chip face to face, vias for service connections.**

(etching to wire bond pads ok)

R&D Issues:

-Technology: compatible with sensor material/ASICs?
-Interconnection quality: e.g. capacitance (face-to-face or die up?).
-Yield & Cost.
-Production in industry (or transfer to HLL).

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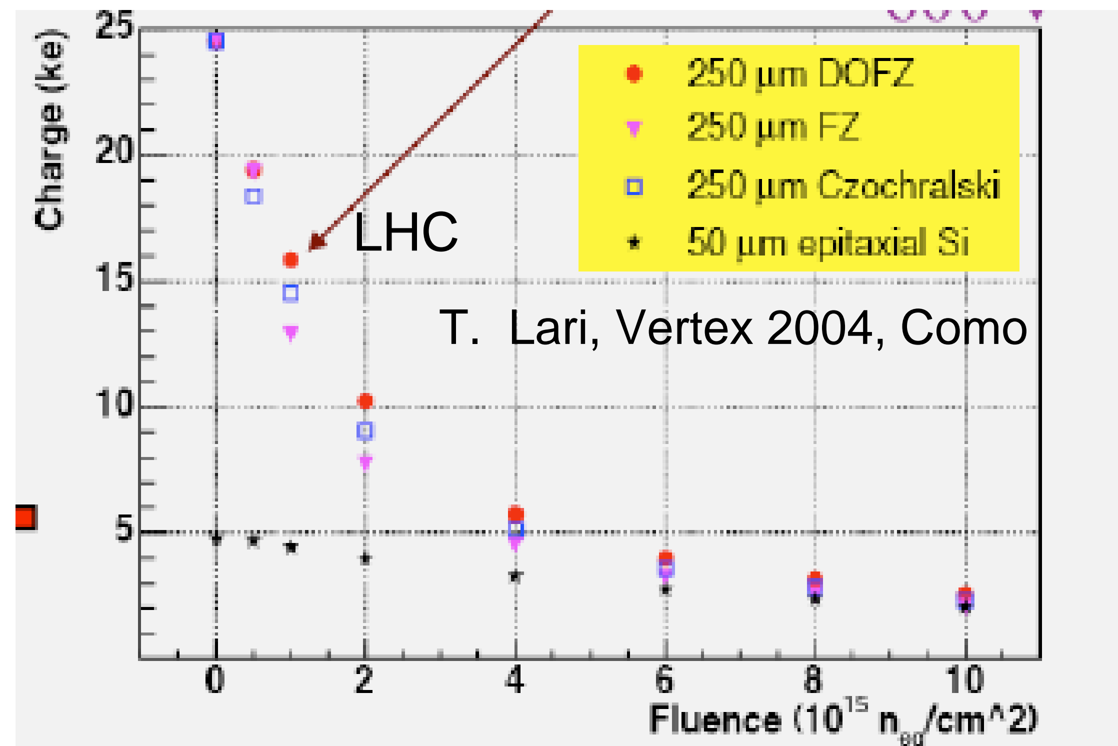
Motivation for Thin Detectors

After 10^{16} n/cm^2:

V_{dep} > 1000V (250 µm) -> operate partially depleted.
Large leakage currents.
Charge loss due to trapping (mean free path ~ 25 µm).
l_e > l_h (need n-in-n or n-in-p) to collect electrons.



No advantage of thick detectors ->thin detectors: low V_{dep}, I_{leak} (and X_0)

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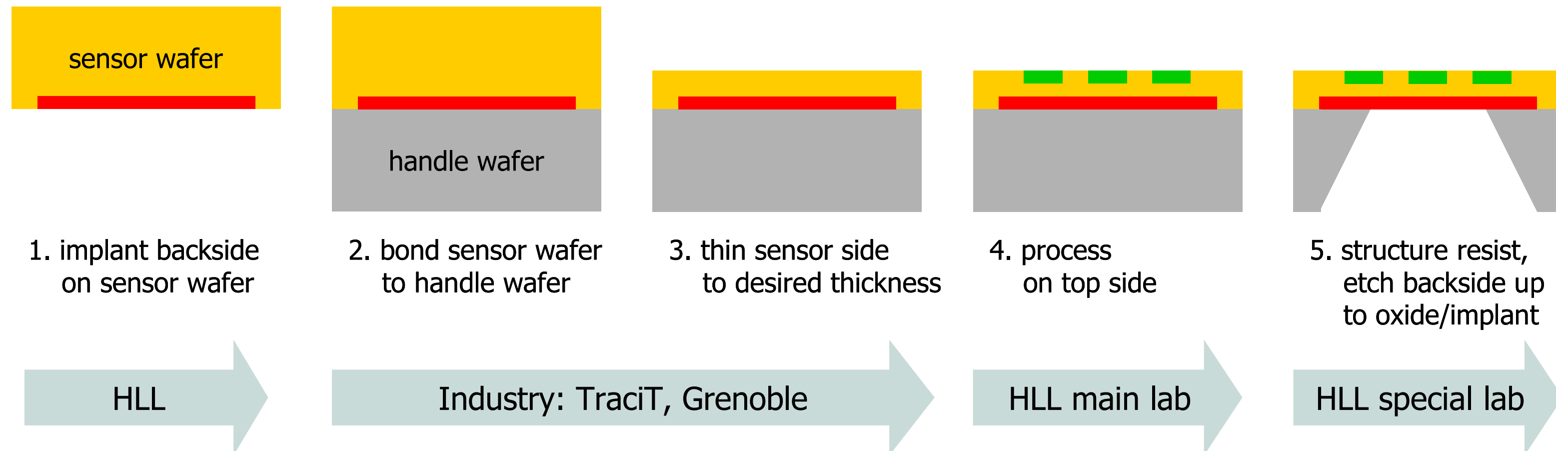
Thinning Technology



- **Sensor wafer: high resistivity d=150mm FZ wafer.**
- **Bonded on low resistivity “handle” wafer”.**

- **Step 1):** **Done in house, could be done in industry.**
- **Steps 2) & 3):** **Done in industry.**
- **Step 4):** **“Perfect” backside protection, even “double sided” (n-in-n) detectors can be processed on single sided lines (industry).**
- **Step 5):** **Done in house, check for industrial process.**

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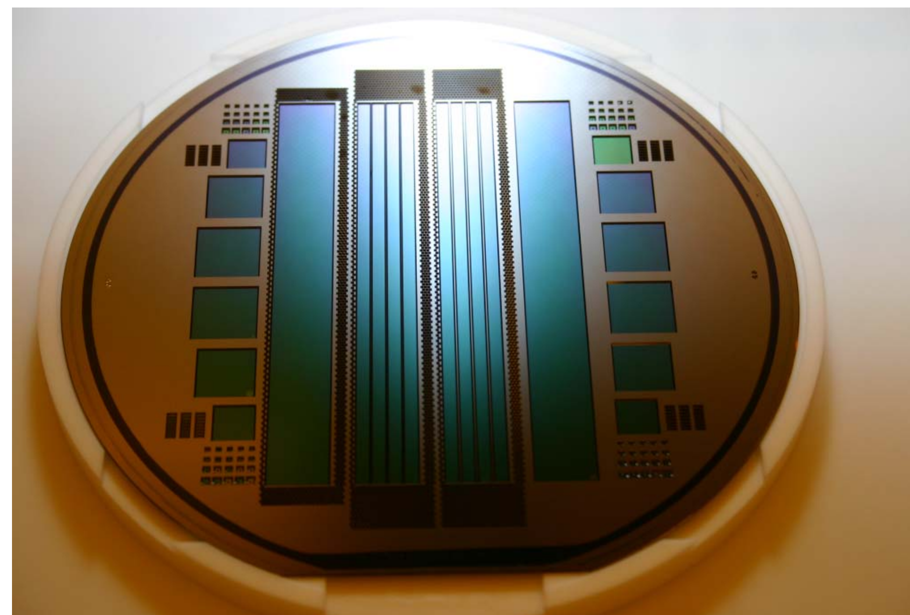
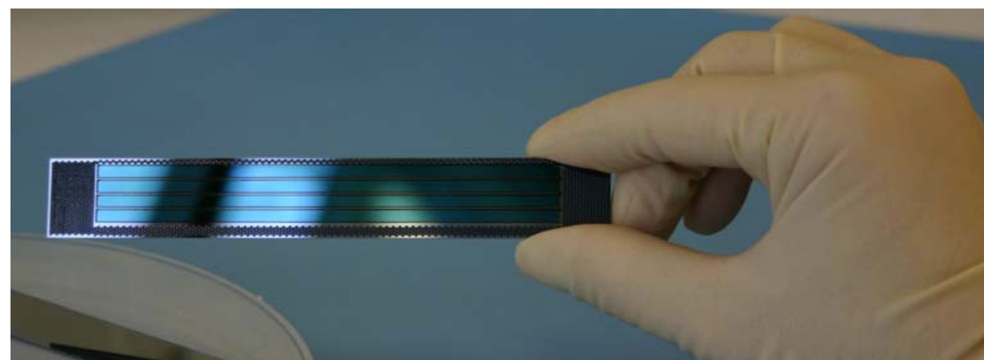
Prototypes

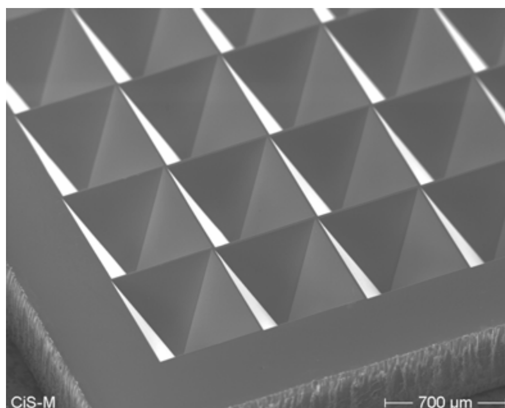
Thin (50 μm) silicon successfully produced at MPI.

- MOS diodes.
- Small strip detectors.
- Mechanical dummies.
  1.3 x 10 cm^2 plus stiffening frame & reinforcement bars.

-No deterioration of detector properties,
keep I_{leak} < 100pA/cm^2







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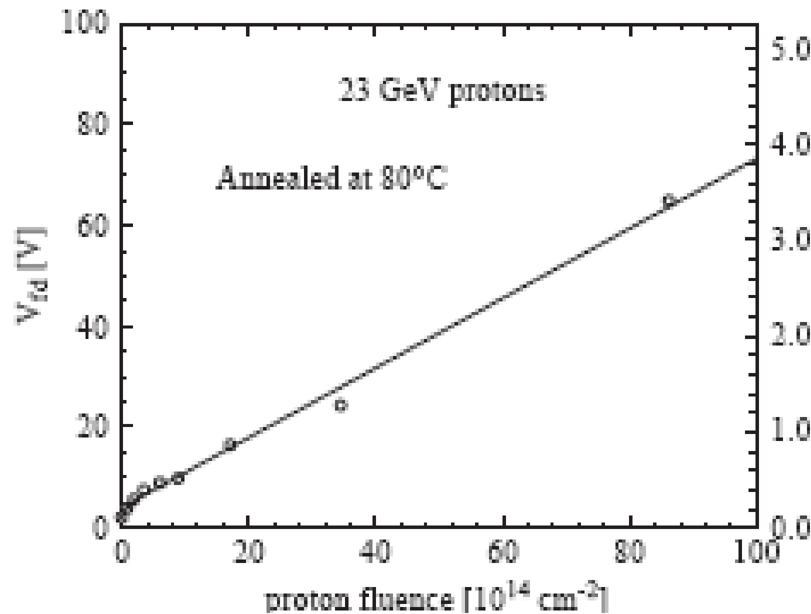
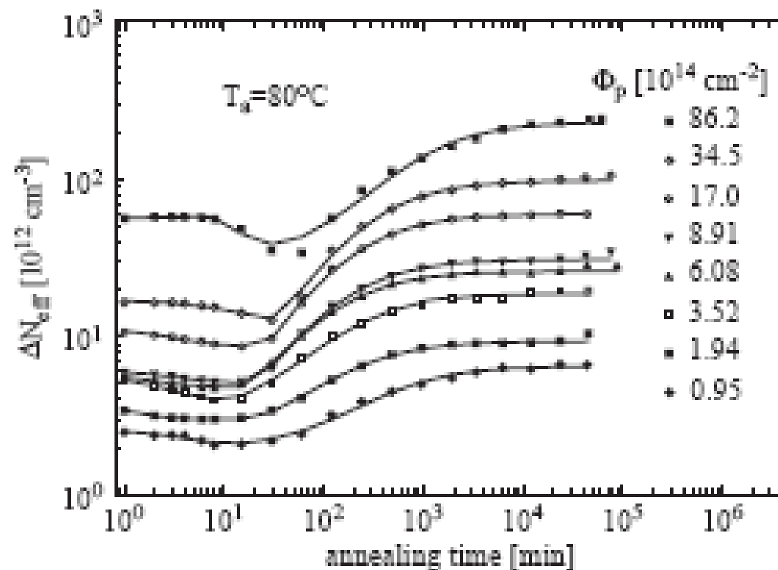
Measurements (V_{dep}, I_{leak})





Fretwurst et al. NIM A 552 (2005):

After short term annealing:

V_{dep} < 100V at 10^{16} 1/cm^2.

However, detectors need to be kept cold (avoid reverse annealing!).

Leakage currents:

α(80°C, 8min) = 2.4 x 10^{-17} A/cm.

Measurements of CCE

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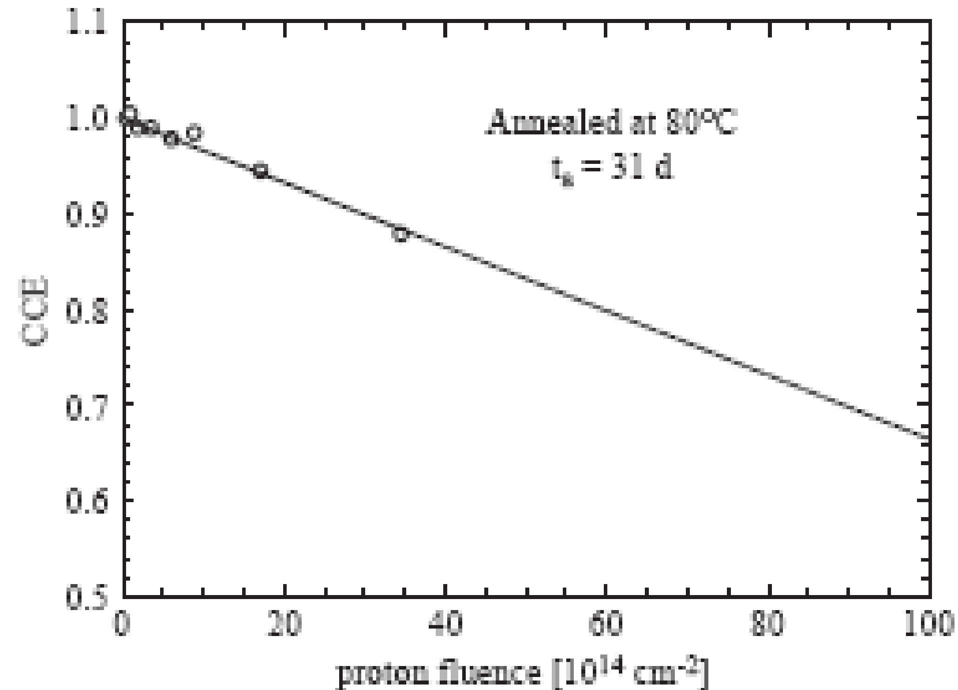

Fretwurst et al. NIM A 552 (2005): MPI diodes, 50 µm:

CCE ~ 66% @ 10^{16} p/cm^2 (extrapolated).

Similar to results from epi-material (G.Kramberger):
3200e (62% average),
2400e (60% most probable).

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Expected Signal/Noise

Item	**Presently 250 μm 50 x 400 μm²**	**thin 50 μm 50 x 200 μm²**	**thin 50 μm 50 x 50 μm²**
$C_{neighbour}$	~300 pF	150 pF	60 pF
$C_{backplane}$	~10 pF	20 pF	5 pF
$C_{interconnect}$	~90 pF ?	??	??
C_{tot}	400 pF	200-300 pF	~100 pF
noise	190 e	~150 e	~50 e
I_{leak}			
pixel 20°C 10^{16}	1.5 μA	150nA	40nA
-7°C	135 nA	14nA	4nA
shot noise:	205 e	66 e	35 e
threshold spread:	50 e	50 e	50 e
effective rms:	**280 e**	**170 e**	**80 e**
Signal (before):	20000 (mp)	4000 (mp)	4000 (mp)
at 10^{16}	~3300	3200 (av)	3200 (av)
		2400 (mp)	2400 (mp)

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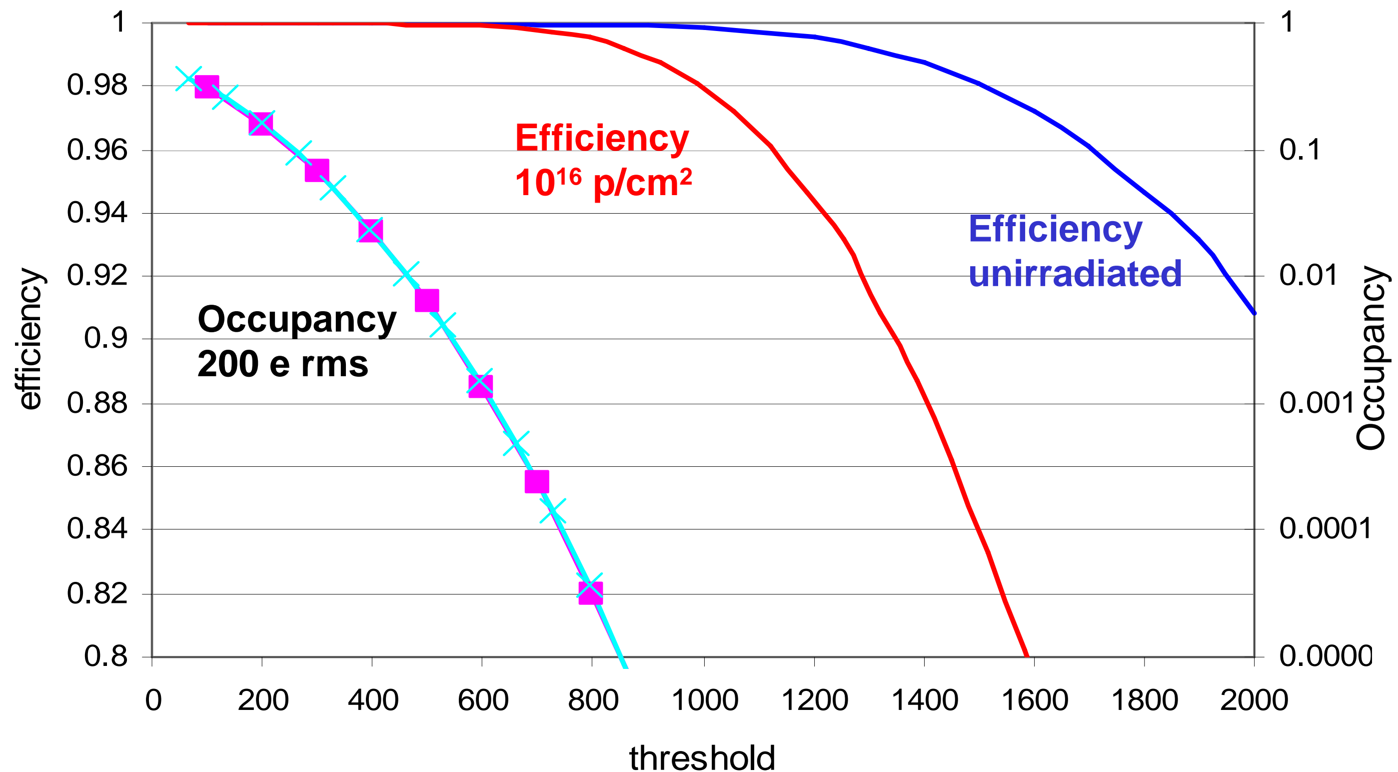
Occupancy - Efficiency

GEANT 4 simulation, 50 µm thick, 50x50 µm² pixel size, physics tracks, diffusion 200e noise (A. Raspiereza):

	average	most probable
Signal with 100% CCE, cluster	4500 e	3300 e
Signal with 100% CCE, max. pixel	3800 e	2800 e
CCE 66%, cluster	2900 e	2500 e
CCE 66%, max. pixel	2500 e	1780 e



Specs: Efficiency: >97% Occupancy < 10^{-5} -> threshold of ~1000 e !

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Summary: Thin Detectors

Cannot beat trapping (with planar detectors) !

- **Keep V_{dep} low.**
- **Keep I_{leak} low.**
- **Reduce X_0*.**

Challenge: small signal!

- **First results on radiation hardness and CCE encouraging.**
- **Can be produced with standard FZ material.**
- **Large scale industrial production possible.**
- **Thickness can be adapted to radius (fluence)**

R&D topics:

- **Make real pixel detectors.**
- **Irradiations, measurement of CCE.**
- **Optimize thickness, n-in-n or n-in-p ?**
- **Optimize production process.**
- **Industrial fabrication.**

***) if this is not an issue: backside etching not necessary, simpler fabrication.**

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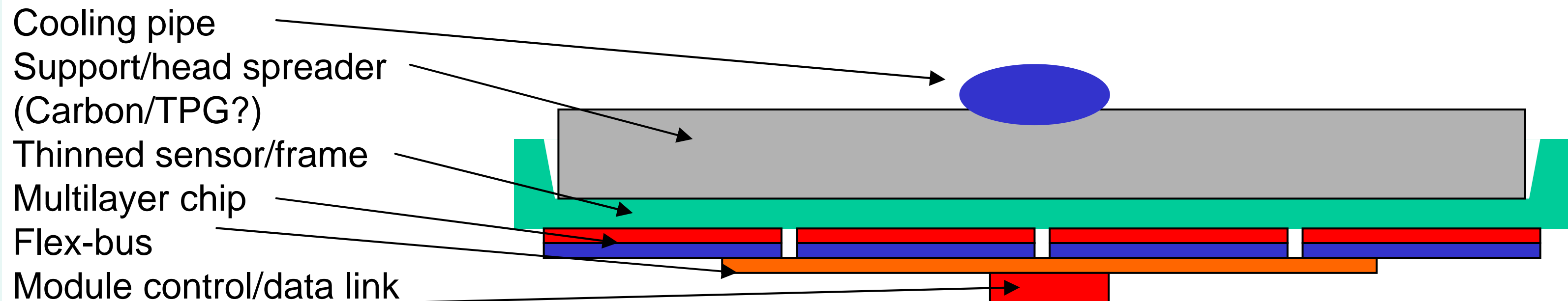
Conceptual Module Design

Work on conceptual module design:

use potential of 3D technology.
reduce material: reduced thickness,
higher integration -> less services.



Cooling of ASIC & Sensor:
~ 100 μm Si ΔT < 10mK for p=50μW/pixel (50x200 μm²).

Material (X_0):

Sensor & ASICs:	**0.12 – 0.26 %**
Carbon/TPG (.5 mm):	**0.2 %**
Flex, MCC,..	**~0.1 %**

	0.42-0.56 % & less support & services

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Summary

We propose an R&D program on:

- 3D interconnection:
  - Alternative to bump bonding.
  - Opening new possibilities for ASIC and module design.
- Thin FZ sensors ("standard" pixel sensors optimized for SLHC).

Modular R&D:

- Thin sensor can be used with standard hybrid pixel AISCs (bump bonded).
- 3D Interconnection is an option for other sensor types (e.g. 3D detectors).

Time Scale:

- Thin Detectors: 2007.
- Simple 3D demonstrator (SLID, no thinning of ASICs): 2008.
- Advanced 3D demonstrator (ICV-SLID, vias, thinning): 2009.

- Resources at MPI: 150 kEuro/year (& one engineer).

Other groups are invited to join (especially ASIC developers).

Radiation Length - SLID-ICV

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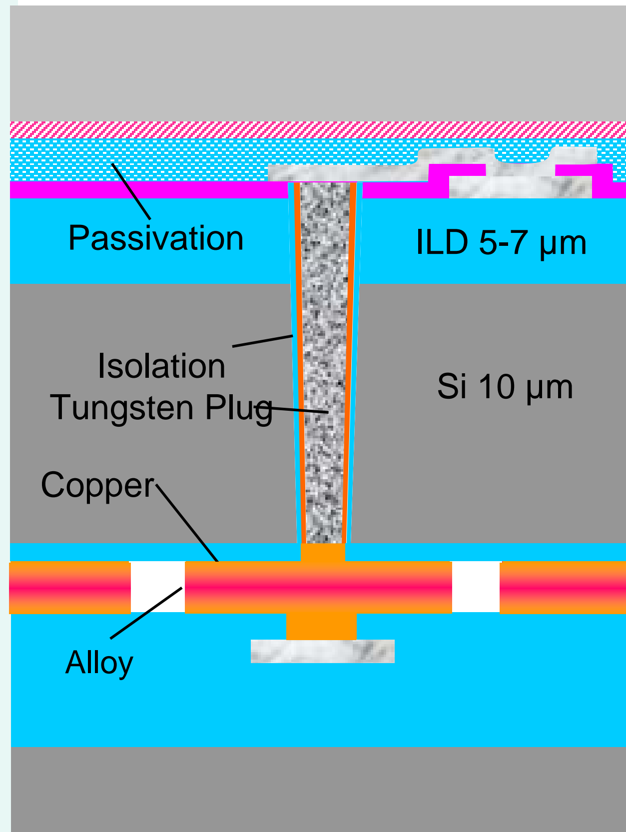


X_0 of

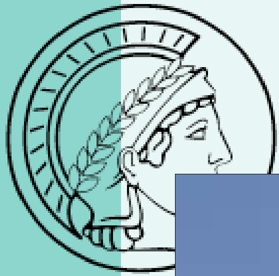
Si: 9.36cm,
W: 0.35cm,
Cu: 1.43 cm,
Sn: 1.21 cm

assuming: -: pixel 50x50 µm², 3 tiers r/o

then material per pixel:

sensor	-:	50…100 µm Si
Si r/o	-: 3x20 µm	60 µm Si
3x ICVs, W	-: 20 µm deep, Φ 4 µm →	8 µm Si
3x contact Cu:	A=100 µm², t=6 µm, →	5 µm Si
3x contact Sn:	A=100 µm², t=2 µm, →	2 µm Si

material per pixel → 125…175 µm Si
0.12-0.16% X_0



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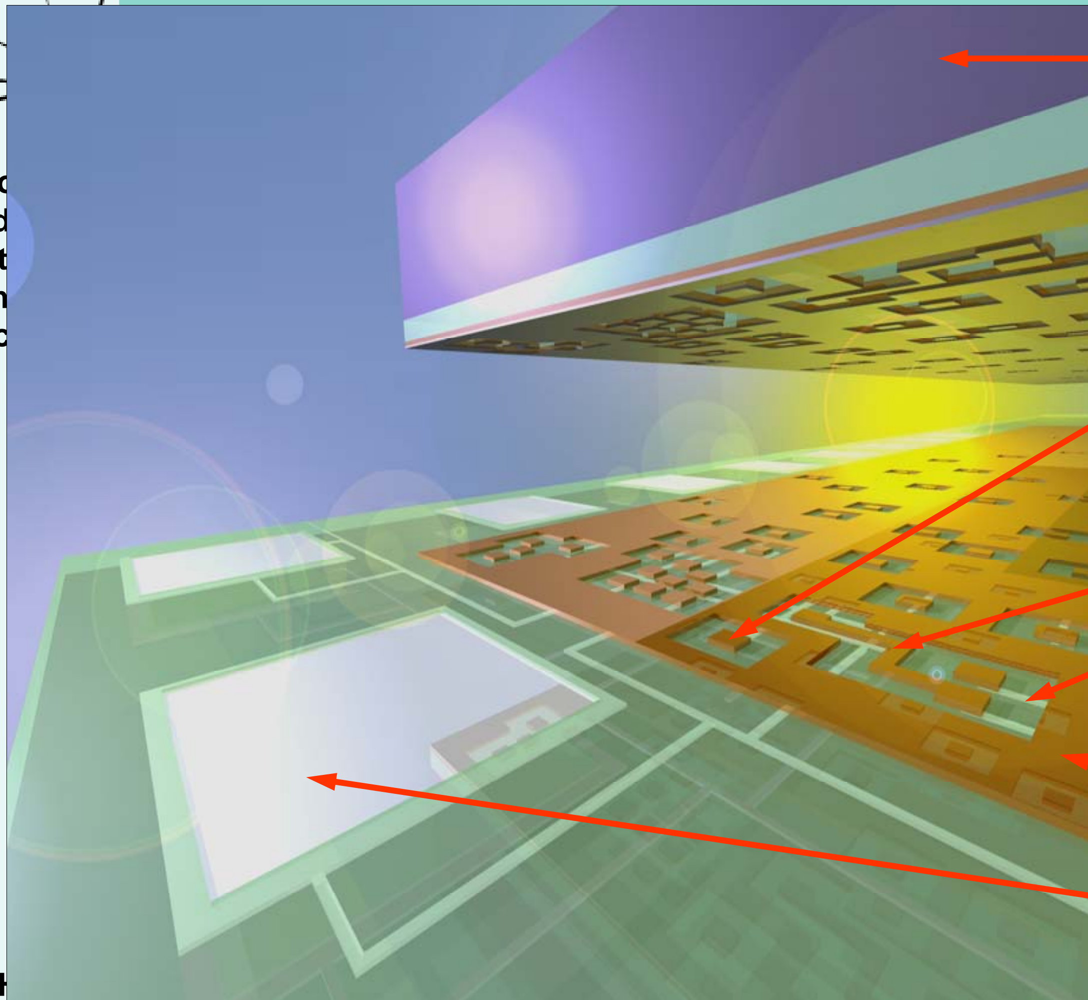
Face-to-Face SOLID Process (IFX)



Top chip
Cu and Sn coating

Bottom chip
Cu coating, bond pads

No underfill

Inter chip vias
15 x 15 µm²
5 µm vias to LM

Redistribution

Insulation trenches
15 µm

Passive area
heat spreader

External IOs
standard wire bonds

Status of the project: Process defined, tooling exists (Datacon, EVG), ready for prodution
unfortunately, Mr. Huebner is now with Qimonda and they don't make chipcards...

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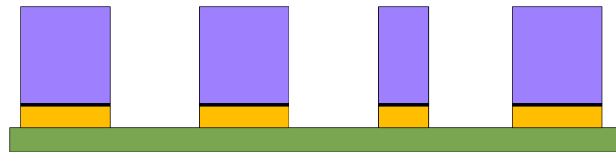
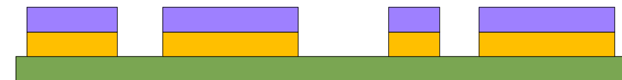
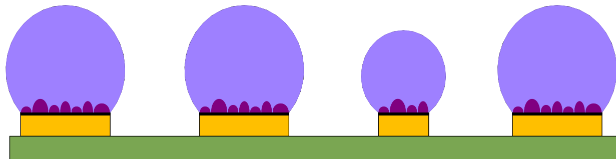
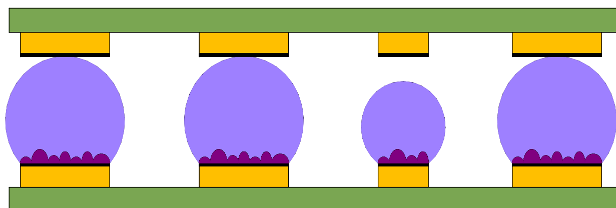
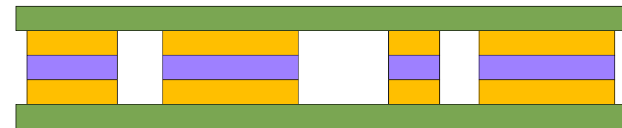
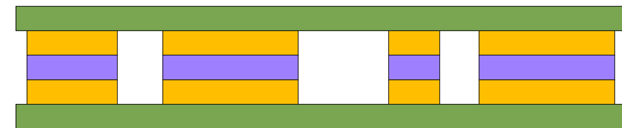
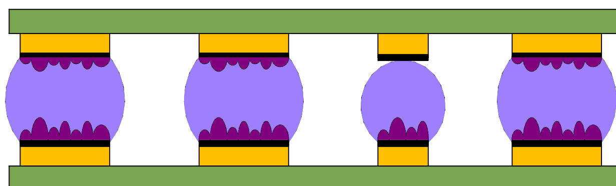
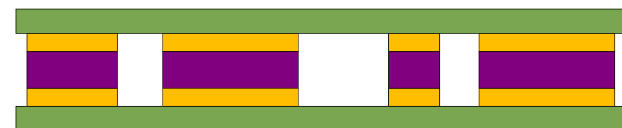
Comparison of Solder Processes

	FBGA	SOLID
1st step	 Metallization and solder apply	 Metallization and solder apply
2nd step	 Reflow	
3rd step	 Pick & place (flux)	  Pick & place (no flux)
4th step	 Soldering	 Soldering

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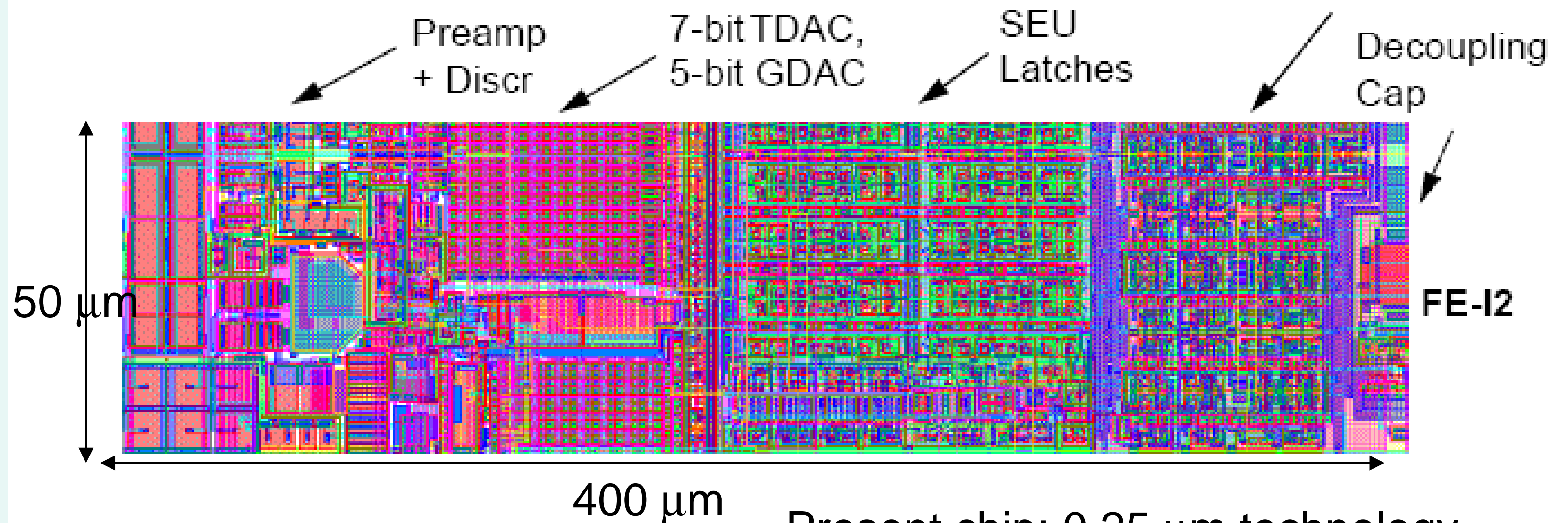
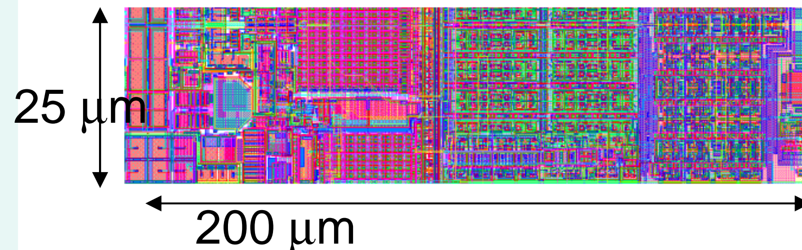
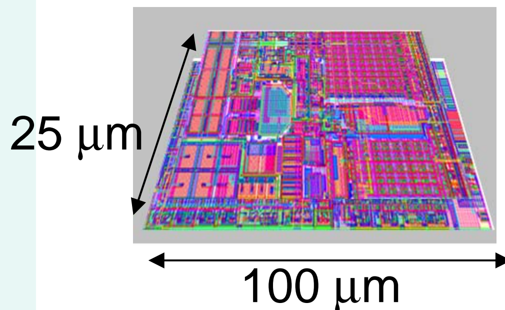
Reduction of pixel size
less capacitance, noise, occupancy



Present chip: 0.25 µm technology



Next generation: 130 nm technology
Reduction ~¼ (area)



½ using 3D interconnection (separation of analog and digital part, for illustration))

Pixel sizes of 25 x 100 µm^2 or 50 x 50 µm^2 possible