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3D Integration of CMOS transistors with ICV-SLID technology

Robert Wieland *, Detlef Bonfert, Armin Klumpp, Reinhard Merkel, Lars Nebrich, Josef Weber, Peter Ramm

Fraunhofer Institute for Reliability and Microintegration, Munich Division, Hansastrasse 27d, 80686 Munich, Germany

Abstract

3D Integration of CMOS transistors with ICV-SLID technology is reported in this paper. NMOS and PMOS metal gate transistor devices have been further processed by forming deep trench inter-chip-vias and by thinning the substrate to 25 μm remaining silicon thickness. No degradation of transistor behavior found due to the additional 3d-processing steps. Results of the process flow and electrical measurements of transistors on thin silicon are shown in this paper.
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1. Introduction

3D integration provides significant performance improvements for micro- and nanoelectronic systems in terms of integration density, multi-functionality and power consumption. Minimal interconnection lengths can be achieved by forming vertical interconnects through thin device substrates within a chip stack.

We present a wafer scale process flow called "ICV-SLID" (Inter-Chip-Via Solid Liquid Inter Diffusion), which is characterized by high density vertical inter-chip wiring of stacked devices and optimized to the capability of chip-to-wafer stacking.

Completely processed Si substrates with active devices such as CMOS transistors have been used for the formation of 3D integrated chip stacks.

2. ICV-SLID technology

Fraunhofer IZM's so-called ICV-SLID technology is based on adjusted Cu–Sn soldering of thinned and vertically metallized device substrates and allows the formation of multiple device stacks. The schematic cross section of a corresponding 3D integrated circuit is shown in Fig. 1. Adjusted soldering on a wafer scale level, using SLID and ICVs, has been reported elsewhere [1,2].

* Corresponding author. Tel.: +49 89 54759 372.
E-mail address: wieland@izm-m.fraunhofer.de (R. Wieland).

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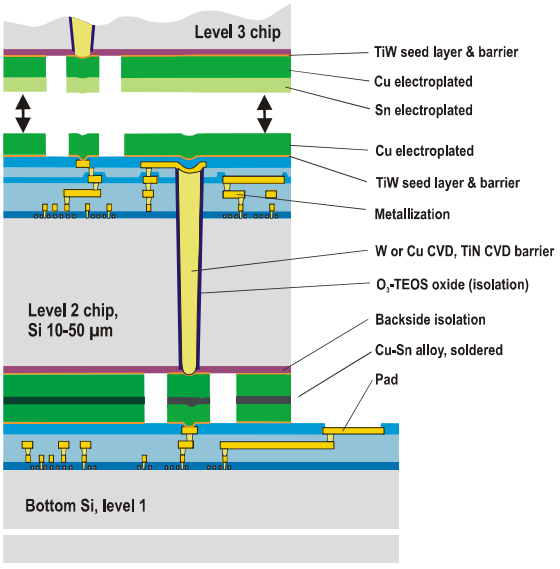

Fig. 1. Schematic cross section of a corresponding 3D integrated circuit with the fully modular ICV-SLID concept.

Fig. 2 shows a corresponding 3D integrated test structure with ICVs and SLID metal system. The thermodynamically stable Cu_3Sn alloy provides the required mechanical and electrical interconnects between the stacked chips or wafers, respectively. Since the Cu-Sn soldering step is the last major process step before the device stack is completed, known feasibility issues due to processing of already bonded wafers, i.e. W- or Cu CVD for ICVs, can be reduced to a minimum.

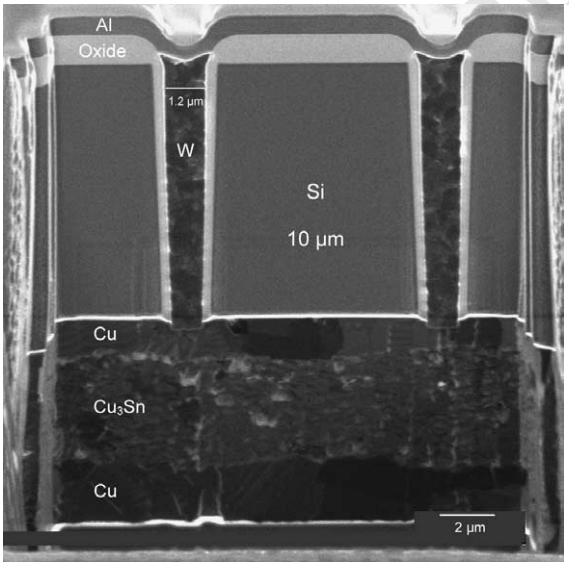

Fig. 2. FIB of a 2-level stack with ICVs and SLID metal system (published in Mater. Res. Soc. Proc. 766, Warrendale, pp. 3-14).

The applied thinning sequence maintains device substrates of approx. 20 µm of remaining Si thickness. Such ultra thin Si-layers can be achieved by using a temporary handling wafer, which holds the thinned device substrate in place. Cu–Sn structures on the backside of the thinned substrate and corresponding Cu structures on the frontside of the bottom wafer are required for the soldering process. After optical alignment, the wafers are soldered using the SLID process and the handling wafer can finally be removed.

3. Experimental and results

Wafer thinning sequences as well as the formation of ICVs are additional process steps that may increase the possibility of failure mechanisms such as stress induced reliability issues or changes of the transistor behavior. In order to study influences of the 3D process flow, suitable test devices containing CMOS transistors were integrated on 200 mm Si wafers.

These wafers were then processed according to the ICV-SLID technology. W-filled ICVs were prepared by etching through all dielectric layers, followed by a 20 µm deep silicon trench etch. For lateral isolation of the ICVs, a dielectric layer was deposited, using highly conformal O_3/TEOS sub atmospheric chemical vapor deposition (SACVD). After depositing a TiN seed layer by metal organic chemical vapor deposition (MOCVD), the ICVs were metallized by using MOCVD of W with a subsequent W etchback step. The minimum lateral distance of the ICVs to transistor gates was approx. 11 µm, the minimal distance to the drain area was 4 µm, shown in Fig. 3. The ICVs were then electrically connected to metal pads by an AlSi1%-Cu0.5% additional interconnect layer, see Fig. 4. Finally, a passivation layer was deposited and the pads were opened.

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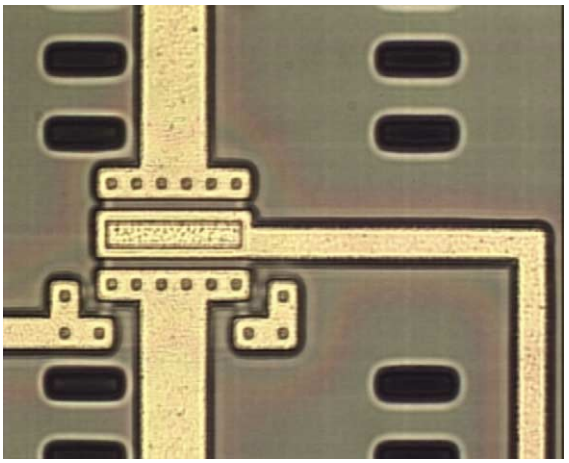

Fig. 3. ICVs after deep trench etching and O_3/TEOS isolation near NMOS transistor.

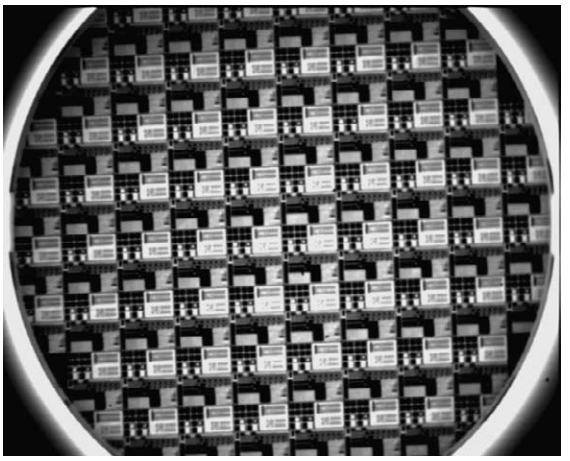

Fig. 5. Infrared transmission of the thinned device substrate, temporarily glued to a handling wafer.

The device substrates were then temporarily bonded to a handling wafer, using a grinder tape as a glue layer, thus allowing for precise thinning by grinding, wet chemical spin etching and dry etching to approx. 25 μm remaining Si thickness, until the ICVs are exposed from the rear. Fig. 5 shows an infrared transmission image of the thinned stack, indicating a defect free temporary bond between the handling wafer and the thinned silicon substrate.

In order to study influences of the thinning and ICV formation process, the device substrate including grinder tape and handling wafer was bonded to a standard Si-wafer by using a spin-on epoxy glue layer. Finally, the handling wafer has been removed by heating the temperature-sensitive grinder tape. Thus, the active test structures on 25 μm thick Si and with ICVs nearby have been successfully transferred without any cracks or defects. A FIB image was taken to check for the integrity of the ICVs, see Fig. 6.

Electrical characterization of the thinned NMOS transistors was done by comparing the transistor behavior with measurements on a reference wafer with standard thickness and no ICVs.

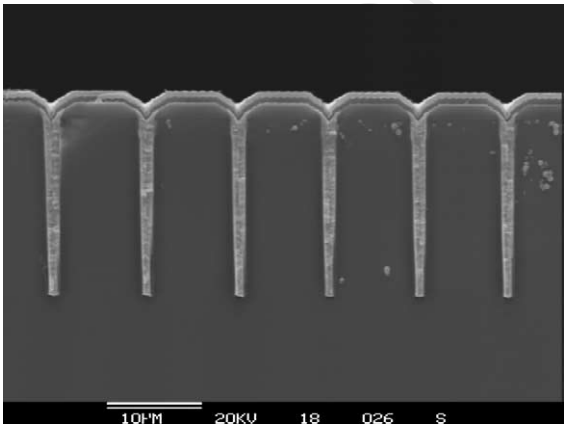

Fig. 4. Test wafer with W-filled ICVs and interconnect metallization.

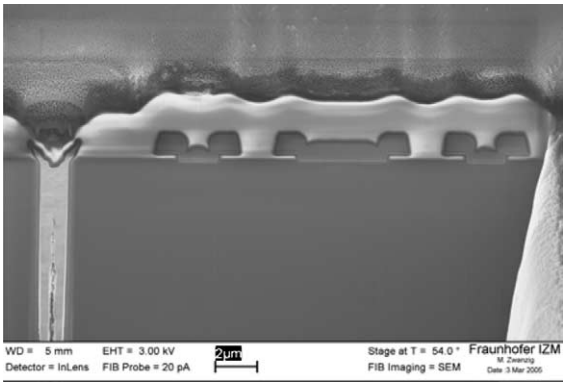

Fig. 6. FIB image of a metal gate NMOS transistor (w/l = 20/2) with W-filled ICV near active area.

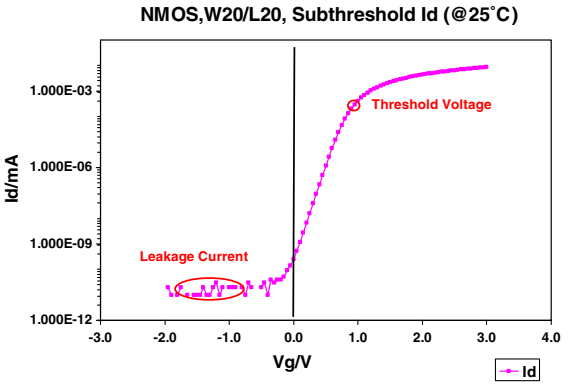

Fig. 7. Transfer characteristics of a NMOS transistor, 25 μm thin Si, minimal distance of ICVs to gate area 11 μm.

Threshold values were taken by use of the extrapolation method.

Single data of typical output characteristics Id (Vd, Vg), transfer characteristics Id (Vg) and threshold voltage were identical with the specifications, compared with the reference wafer. Fig. 7 shows a typical transfer characteristic of a metal gate NMOS transistor.

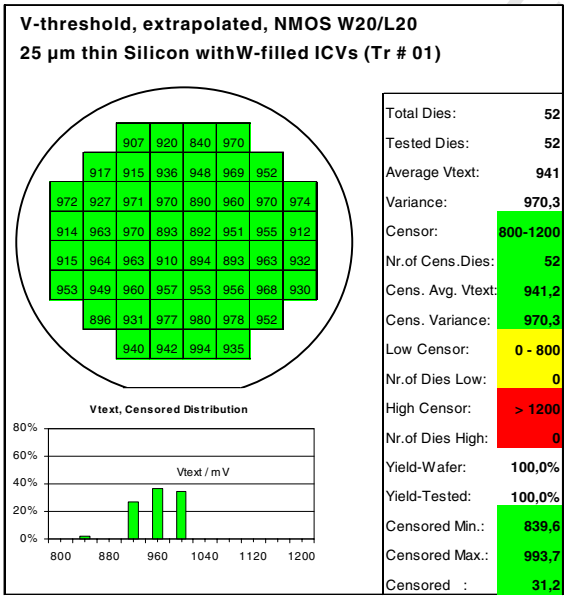

Fig. 8. Wafer map of V_{thr} for a NMOS transistor after preparation for 3D Integration with W-filled and isolated ICVs on 25 μm thin Si.

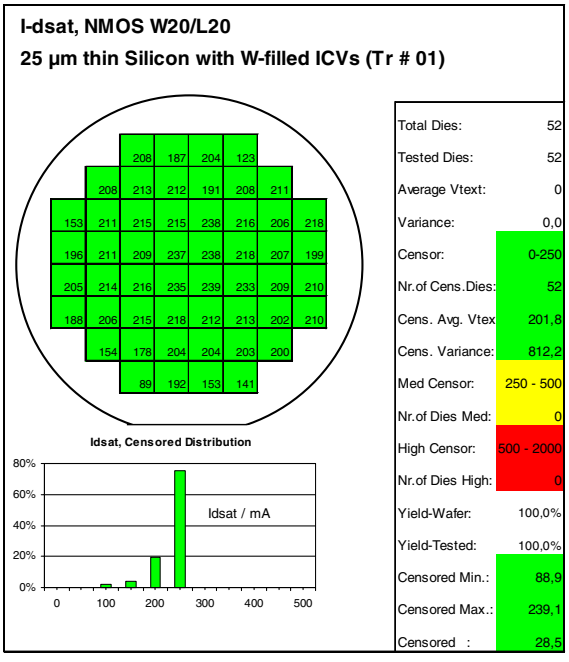

Fig. 9. Wafer map of I_{dsat} for a NMOS transistor after preparation for 3D Integration with W-filled and isolated ICVs on 25 μm thin Si.

Wafer maps were taken of three different transistors: not thinned reference wafer, thinned wafer without ICVs and thinned wafer with ICVS near the transistor. In all cases, the extrapolated threshold voltage was in the range of 919–941 mV, and the drain saturation current was in the range of 223–201 mA, respectively. Corresponding wafer maps are shown in Figs. 8 and 9.

In order to check the isolation of the ICVs to the top silicon, resistance measurements were taken by applying a DC voltage between the pads of the ICVs and a nearby Si-bulk contact. At a DC voltage of 20 V, the leakage current was in the range of 200 fA (typical measurements).

A wafer map was then generated with a DC voltage of 25 V, resulting in an average leakage current of 90 pA, shown in Fig. 10.

A higher current can only be observed in the center of the wafer, the edge areas are still in the fA range. This effect might be due to a reduced thickness of the O_3/TEOS isolation layer at the top of the ICVs in the wafer center, caused by the known non-uniformity of the W-overetch step.

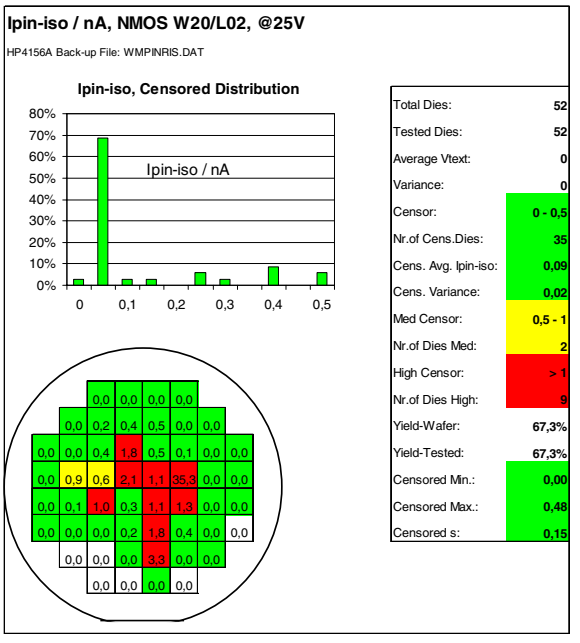

Fig. 10. Wafer map of $I_{ICV\ isolation}$ for 20 μm deep ICVs, isolated to the Si-substrate with approx. 260 nm O_3/TEOS SACVD.

4. Conclusion

Influences on active test devices induced by the 3D integration process have been studied. Completely fabricated CMOS transistors were processed using the ICV-SLID technology for 3D integration, including wafer thinning down to 25 μm and the formation of W-filled inter-chip vias as "through silicon" electrical interconnects. The 25 μm thin silicon wafers were finally glued to a Si-substrate by use of an epoxy layer.

Electrical measurements, including wafer maps of threshold voltage and drain saturation current, showed no impact of the ICV-SLID process on the transistor behavior.

Sufficient electrical isolation of the ICVs to the top bulk silicon was found with leakage currents of <200 fA at 20 V.

Acknowledgement

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