	R&D on a novel interconnection technology for 3D integration of sensors and electronics and on thin pixel sensors		
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R&D Proposal for the SLHC

R&D on a novel interconnection technology for 3D integration of sensors and electronics and on thin pixel sensors

Abstract:

We present an R&D programme towards a novel pixel module concept. As an option to replace the bump bonding process, the pixel sensor will be connected to the read-out electronics by the novel Solid-Liquid InterDiffusion (SLID) interconnection process developed by the Fraunhofer-Institut IZM, offering finer segmentation and potentially lower cost. In addition, using ICV-SLID, namely Inter-Chip Vias together with the SLID process, allows for a compact design, i.e. a higher live fraction and eventually for the vertical integration of analog and digital electronics made from different chip technologies. The interconnection technology will primarily be developed in conjunction with planar, radiation tolerant, thin pixel sensors, which will be 50–100 μm *thin and produced using a wafer bonding technology, but also be applied to other sensor types. This pixel module concept opens new possibilities for the optimisation of radiation tolerance, power consumption, speed and complexity.*

Prepared by:	*Checked by:*	*Approved by:*
Richard Nisius (nisius@mppmu.mpg.de), Hans-Günther Moser (hgm@hll.mpg.de)		

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A	19/01/07	All	R. Nisius	Original document submitted to the HLSG
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Contents

1 Introduction

The requirements for the inner detector upgrade and the options considered are given in [1]. Within the inner detector upgrade, the pixel detector upgrade is the most challenging part for what concerns the detector segmentation and radiation tolerance of both the sensitive material and the electronics.

The long term planning foresees a luminosity upgrade of the LHC, the SLHC, to start operation in about 2016. At the SLHC the particle rates and integrated radiation levels are expected to be about a factor 5–10 higher than at the LHC. The rough estimates are about 5–10k tracks per event, an instantaneous luminosity of $L = 10^{35}/\mathrm{cm/s}$, and an integrated luminosity of $\mathscr{L}_{\mathrm{int}} = 2500\,\mathrm{fb}^{-1}$ for 5 years of operation. The expected 1 MeV neutron equivalent fluence at the innermost radius of the pixel detector will accumulate to about $\Phi_{\mathrm{eq}}(4\mathrm{cm}) = 1.6 \cdot 10^{16}/\mathrm{cm}^2$. On the way to the SLHC detector there will be an intermediate step taken, the upgrade of the B-layer, which is planned to be installed in 2012. Within ATLAS the R&D needed for this intermediate step has started, including R&D on the CMOS detector electronics [2]. The readout of the present pixel detector which is made in 0.25μ CMOS technology, has to be replaced by electronics based on the 0.13μ or even the 90nm technology [2]. This should improve radiation tolerance as well as integration density. The planned R&D described here will be conducted within the overall ATLAS upgrade programme in close collaboration with other interested institutes, making use of the expected advances in CMOS electronics mentioned above.

The choice for the inner detector at the SLHC has been made for an all silicon solution with decreasing granularity for increasing radius. Although the general strategy is clear, the details of the layout and the module concepts to be used at various radii are still open [1]. Especially the radial extension of the pixel detector is still under discussion, and this decision will be very much influenced by the cost. One of the largest cost driver for the present pixel modules is the bump bonding. Consequently, improvements to reduce the cost for this process, or the development of other solutions are highly desirable. In the proposed R&D we will investigate the applicability of a new industrially pursued concept for 3D integrated circuits based on a novel process developed by the Fraunhofer-Institut (IZM) [4].

After irradiation at the SLHC the performance of the present generation of pixel sensors would be severely degraded by too large depletion voltages required, large leakage currents and severe charge trapping. Therefore, several improvements to planar sensors, as well as completely new technologies, are being investigated. Amongst them are thin planar sensors (where the implants are flat areas at the surfaces), and 3D-detectors [3] (where the implants are oriented across the entire bulk). This R&D programme aims at improving the properties of planar sensors. Based upon the experience of the MPP semiconductor laboratory, HLL, with the fabrication of thin silicon sensors, we have started to investigate the feasibility of a novel module concept for the pixel region, by combining the good features of thin sensors, i.e. low depletion voltage and large charge collection efficiency (CCE) even after high radiation doses, with the novel interconnection technology.

A schematic view of a combination of the two technologies for a possible application as a pixel detector module for the SLHC is shown in Fig. 1, see [5]. Ideally, in a final layout, from bottom to top the module comprises a module control chip (MCC), a flex bus, a layer with digital electronics for control and temporary data storage, a layer with analog electronics for signal processing, and the sensitive device consisting of a planar 50–100 μm thin silicon sensor segmented with pixels, together with its frame provided by the remainder of the Handle Wafer used during sensor fabrication (see below). In addition shown is a module support structure combined with a heat spreader connected to the cooling pipe. The heat spreader may be made from a carbon-carbon substrate or from thermal pyrolytic graphite (TPG) [6].

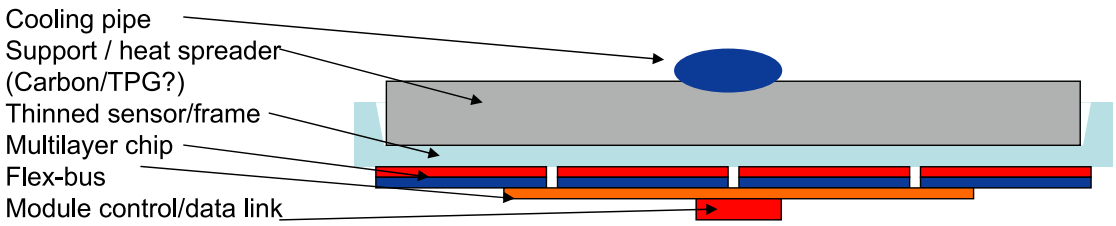

Figure 1: Schematic view of a novel pixel detector module for the SLHC. The module width is about 3 cm.

The main advantages of such a device would be radiation tolerance, i.e. low depletion voltage, low leakage current, and highly efficient charge collection due to the small depleted volume. In addition, the novel high density interconnection technology allows for smaller pixel sizes than in the current ATLAS hybrid pixel detector, which may be hard to achieve by the presently used bump bonding technique [7]. A smaller pixel size will result in a lower capacitance even for thin sensors, giving lower noise and consequently a high signal to noise ratio.

The overall thickness of the sensor and the electronics can be made smaller than 150 μm giving a preferable material budget compared to present devices, thereby keeping the radiation length small. At present sensor and electronics make up about 25% of the total average radiation length of a module. A rough estimate for the thin device gives an average radiation length of 0.11–0.16% X_0 for the sensor and electronics, to be compared with 0.46% X_0 for the present pixel module. The 3D integration avoids the presently used cantilever of the ASICs. The 3D integrated chips are 4-side buttable such that a very compact layout with much reduced dead regions can be realised. In addition, it allows for the independent optimisation of the analog and digital readout electronics.

To arrive at such a detector several aspects have to be thoroughly investigated with extensive R&D. This proposal concentrates on two areas, the 3D integration of sensors and electronics (Section 2), and the development of thin sensors (Section 3). We warmly invite collaborators to join in both areas, and particularly also in the development of new readout electronics, which is not yet covered in this proposal, to make use of the full potential of the 3D integration concept.

2 3D integration of sensors and electronics

The assembly of 3D integrated circuits is an industrially promoted vertical integration concept for electronic devices in which several interconnected layers are arranged on top of each other rather than side by side, offering the possibility of a considerable reduction in circuit overhead on the chips, thereby making them faster. The 3D integrated circuits are discussed in the International Technology Road-map for Semiconductors [9], and investigated by industry as one way to permit the continuation of Moore's Law. Several 3D integrated prototypes have already been realised [10]. However, as of today, no silicon sensor used in high energy experiments has been connected this way. The R&D proposed here applies this technology to a pixel module with emphasis on the simplification of the module design, performance, and reduction of production costs.

Problems of the present pixel module are the high costs for bump bonding and the limitation in segmentation inherent to the bump bonding process. Here these issues will be addressed by a novel interconnection technology called SLID (Solid-Liquid InterDiffusion). Another unwanted feature of the present pixel detector is the moderate live fraction of about 71% related to the design of the

sensors as well as the electronics [2]. One way out is offered by the 3D integration concept using the ICV-SLID process (Inter-Chip Via together with the SLID process). This ultimately also allows for further optimisation in performance and cost by designing the analog and digital parts of the electronics using different technologies. The interconnection and 3D integration will be discussed in turn.

The sensors and electronics will be connected using the novel SLID interconnection technology [11], developed by the IZM, offering a higher density and potentially lower cost alternative to bump bonding. In short, in the SLID interconnection process, the sensor and electronics will be covered by a TiW layer acting as diffusion barrier. Then a thin Cu layer is applied by electroplating to both the sensors and the electronics followed by a Sn layer which is electroplated only to the sensor. Finally, the sensor and electronics are brought together and heated such that an CuSn alloy is formed which makes the interconnection. The alloy is stable up to much higher temperatures than are needed to produce it, which makes it possible to apply the SLID process successively to several layers of integration. At the IZM the interconnections can be made either wafer-to-wafer, or die-to-wafer [12], thereby decoupling the yield for chip production. From the results of the IZM a pixel length of 20 μm seems well possible. In addition, using SLID would also address the issues of radiation hardness by allowing smaller pixels, thereby reducing the pixel capacitance and hence the noise. A smaller pixel size is eventually needed to compensate for the loss of resolution due to reduced charge sharing in sensors with thin active layers. A smaller pixel size has the additional benefit of an improved two track separation, which may be useful due to the hight track density at SLHC.

Besides the interconnection of chips and sensors this technology allows for 3D integration of thinned chips with through silicon vias by using the ICV-SLID process. At present these vias can be made with a cross-section of about 2×2 μm squared and an aspect ratio of about 8. They are filled with a diffusion barrier discussed above and with Cu or W. A typical resistance of a via including SLID is about 2.5 Ohm. Experience from IZM shows that no significant impact on the chip performance, i.e. on MOS transistors close to the vias, is observed. The ICV-SLID process could already be used to connect the services from the back rather than from the side for a detector made from a sensor attached to a single layer of electronics. Through vias would allow for a 4-side buttable module layout, i.e. no cantilever of chips would be needed and modules would not be limited to two rows of chips, the dead space for routing would be minimised, simpler services could be made and less material would be needed.

In a final step the ICV-SLID process opens the possibility for 3D stacking of electronics made from different technologies. Different functionalities, like analog amplification, digital control and readout, can then be realised in different ASIC technologies and integrated into one monolithic device. These different technologies can be optimised individually in terms of speed, power and radiation hardness allowing for a better overall performance. Clearly such an advanced multi-layer ASIC is more challenging in terms of circuit design, testability of ASIC (components), and yield. However, a first step using only a single layer ASIC with through silicon contacts form the backside would need only moderate changes to traditional ASIC design and fabrication.

In this proposal the 3D integration will primarily be developed using the well advanced technology of thin FZ sensors. However, it is not restricted to this, and the applicability to the presently developed 3D-detectors will also be studied.

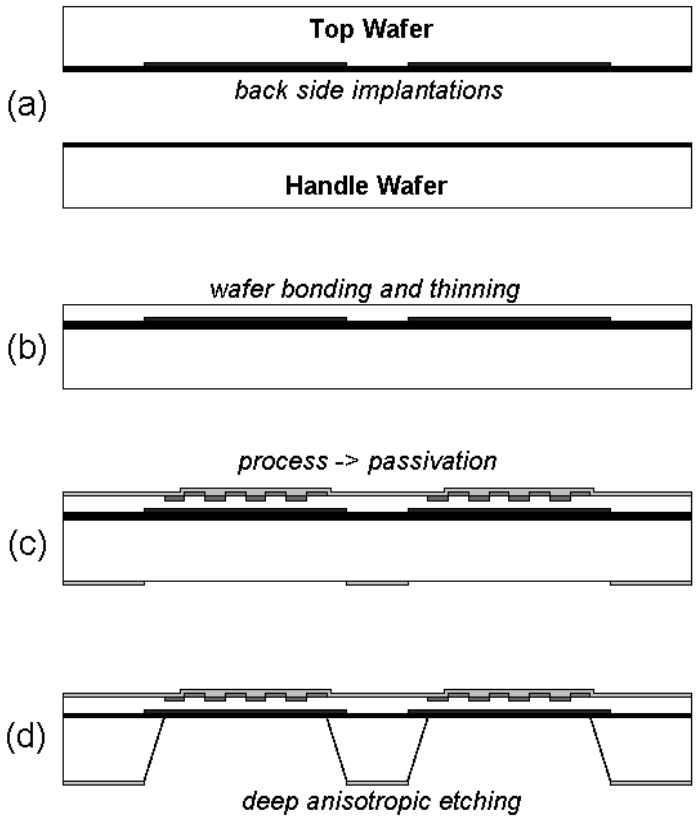

Figure 2: Production steps for a thin pixel sensor for the SLHC.

3 Development of thin pixel sensors

Based on the good experience with the R&D on thin DEPFET detectors [14] for the International Linear Collider project we intend to further develop the wafer bonding technology together with the deep anisotropic etching process for the fabrication of 50–100 μm thin pixel sensors for SLHC.

In highly irradiated silicon, the charge collection efficiency is reduced due to trapping resulting in an active thickness of the sensors of 50 μm or even less. This means that for presently used sensors of about 300 μm thickness, the signal is only collected from a very small part of the sensor. Depleting the full sensor thickness leads to unacceptable depletion voltages at the large fluence expected at the SLHC. For example, at a fluence of $\Phi_{\mathrm{eq}} = 10^{15}/\mathrm{cm}^2$ present 300 μm thick sensors are fully depleted only at several thousand Volt, whereas for thin sensors it was shown that they are fully depleted already at less than 100Volt, albeit at a ten times higher fluence, see e.g. [15]. Although, operating the present sensors at lower voltages, i.e. partially depleted, is possible, achieving the same collected charge [16] at a much reduced depletion voltage compared to present sensors is a clear operational advantage of thin sensors.

Thinning the sensors does not overcome the problem of small signal sizes, which will be challenging for the electronics, but it significantly reduces the problems caused by large leakage currents and high depletion voltages, and on top of this, considerably reduces the radiation length of the sen-

sor. The small signal needs to be compensated by excellent low noise electronics and/or a reduction in pixel size which can be achieved with the interconnection technology described in Section 2. The most difficult part is to achieve a low in time threshold of the electronics, a problem which might be considerably reduced if the SLHC will be operated with 50 ns bunch crossing time, which at present is the preferred option [13].

Another challenge of planar detectors with small active thickness is the reduced charge sharing between adjacent pixel which may lead to a degraded resolution compared to thick sensors. This could be compensated by inclining the sensors or, eventually, again by reducing the pixel size.

Thin sensors can be fabricated both in n-in-n or p-in-n technology, on float zone (FZ) material. The thickness is a parameter which can be optimised within a wide range. The process is described in detail in [14] and depicted in Fig. 2. It uses two oxidised wafers, where the oxide layer is needed as a barrier to stop a deep anisotropic etching process that provides the means to remove most of the silicon of the inactive layer. In short, starting from two oxidised wafers, the Top Wafer is processed from the back side, Fig. 2(a), wafer bonded to the Handle Wafer, thinned to the desired thickness, Fig. 2(b), and processed and passivated from the top side, Fig. 2(c). As a by-product of the wafer bonding process the Top Wafer will automatically be oxygenated, thereby improving the radiation hardness [17]. Finally the Handle Wafer is thinned from the backside using a deep anisotropic etching process, Fig. 2(d). A big advantage is that the whole sensor processing sequence can be done on standard production lines. In addition, for the top side processing, this concept offers perfect backside protection, hence double sided detectors (e.g. n-in-n) can be processed on standard single sided processing lines.

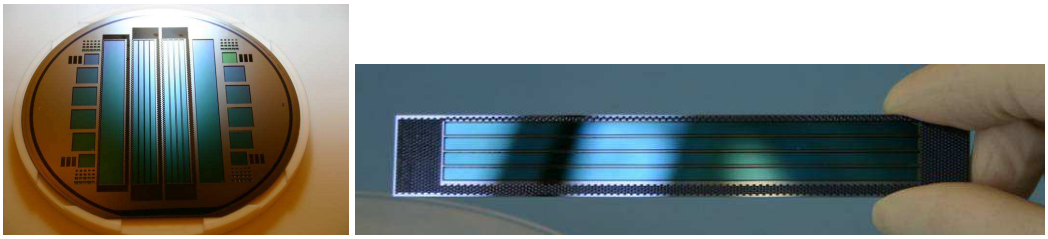

Figure 3: Prototype production of thin FZ sensors. Shown are the wafer layout (left) and a large scale mechanical sample (right).

Simple 50 μm thin small test diodes from n-type FZ material, together with large scale (1.3×10) cm^2 mechanical samples, have been manufactured at MPP. Fig. 3 shows a wafer on the left side and on the right side a large scale mechanical sample, where the support frame leftover from the Handle Wafer is clearly visible. The thin diodes have been irradiated, and their performance has been studied [15]. As examples, the depletion voltage, and the charge collection efficiency both as functions of the fluence are shown in Fig. 4. An excellent performance is demonstrated with a depletion voltage, V_{fd}, of only about 70 Volt at a proton fluence of $9 \cdot 10^{15}/\mathrm{cm}^2$, and a charge collection efficiency, CCE, of well above 85% at a proton fluence of $3.5 \cdot 10^{15}/\mathrm{cm}^2$.

This part of the R&D programme provides an alternative to other developments like EPI material [18] or 3D-detectors [3]. The aim is to develop rather conventional detectors which can be made by industry in large numbers at relatively low cost, which however overcome most of the operational problems of present thick detectors, namely high depletion voltage, large leakage currents and the danger of thermal runaway. Although we aim for using the thin sensors together with the novel SLID interconnection technology described below, the sensors would be fully compatible with the

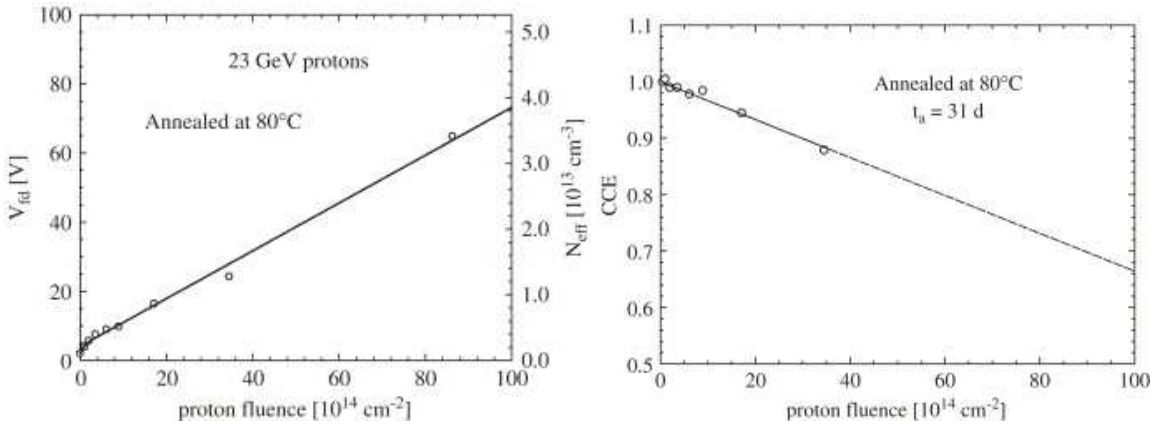

Figure 4: Performance of 50 μm thin diodes as a function of the proton fluence. Shown are the depletion voltage, minimal V_{fd}, after 8 min annealing at 80^{o}C (left), and the charge collection efficiency (CCE) after annealing 31 days at 80^{o}C (right) [15].

presently used bump bonding technology. The main R&D work on thin sensors is to produce real pixel sensors, irradiate those, study their performance, particularly the charge collection efficiency, and the charge sharing for various pixel dimensions, and finally decide for the technology, either n-in-n or p-in-n. Further tasks are the optimisation of the sensor thickness and the production steps, and finally the transfer of the etching technology to industry.

4 Time planning and resources

The aim of the planned R&D up to and including the year 2009 is to arrive at a working prototype consisting of a thin planar sensor and a single layer of electronics using the existing pixel chips connected by the SLID process and using a backside contact with the help of a through via, Fig. 5, thereby demonstrating the usability of the basic features of this new technology. Since, at present, the availability of already produced pixel chips is very limited due to their possible use for the b-layer upgrade, we will participate in a new production run. In parallel the compatibility of the SLID process with the 3D-detectors will be investigated.

To achieve these goals, we have identified a series of steps to be successfully performed within the time periods listed in Table 1. In the first step, which has been started beginning of 2007, we investigate the compatibility of the interconnection technology with the silicon sensor technology. For this, wafers containing simple diodes have been made at HLL. We prepared the sensors for the interconnection process by creating flat surfaces, and included diffusion barriers to protect the sensor edges from penetrating ions from the SLID process, namely Cu. Measurements of the IV-characteristics of the diodes after applying the TiW barrier as well as a Cu layer did not show any significant deterioration. The sensors will now be subject to the full SLID temperature cycle at IZM and afterwards wafer properties like IV characteristics and flat band voltages will be measured again. In parallel, thinned diodes, as well as mechanical sample detectors to investigate the mechanical rigidity of the samples, will be fabricated. Irradiation hardness of the diodes, i.e. the operation voltage, reverse annealing and trapping will be investigated in close collaboration with other groups within the RD50 [8] framework. Then a series of steps is foreseen to successively

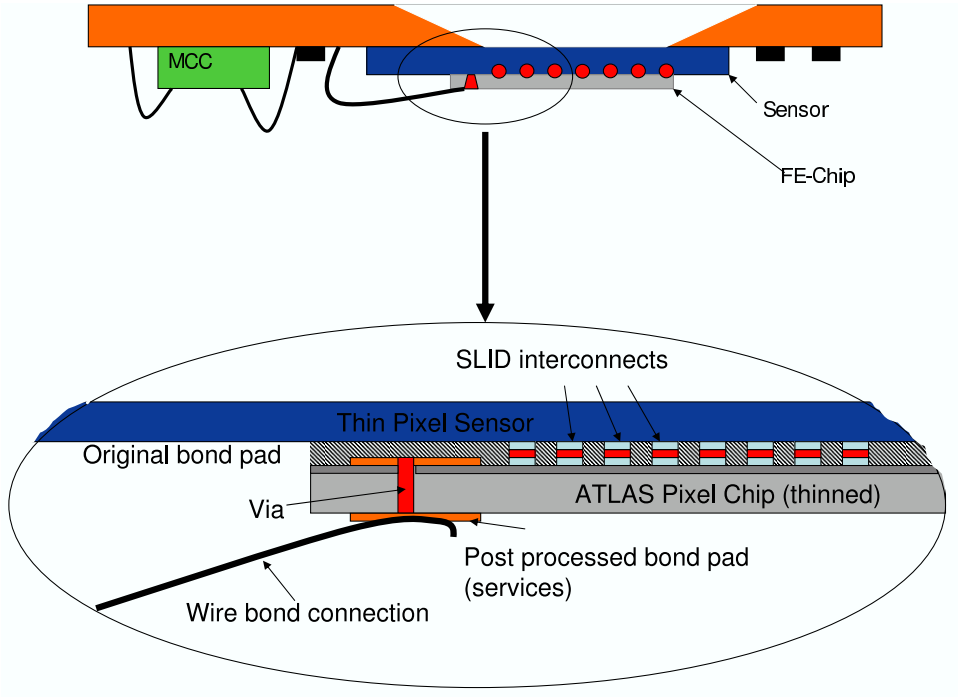

Figure 5: Example of a prototype module using the ATLAS pixel chip and a thin sensor integrated using the ICV-SLID technology.

arrive at a prototype module built using the ICV-SLID process on an existing ATLAS pixel chip and a thinned pixel sensor. For this, eventually also the ATLAS chip will be thinned and services will be connected using through inter silicon vias. A possible layout of such a prototype module is shown in Fig. 5. In this example the ATLAS chip is connected face to face to the sensor while the service contacts are made from the backside using wire bonds attached to bond pads on top of through vias.

This R&D will be conducted by the Universities of Bonn [19], Dortmund [20] and Oslo [21], Interon [22], and the MPP Munich [23]. The activities of the various institutions are listed in Table 2. The technical staff presently dedicated to this project are 1 FTE process engineer, 1 FTE mechanical engineer, 1 FTE mechanical technician at MPP. Oslo also contributes with their workshops if needed. The MPP allocated budget amounts to 170 kEuro per year for an initial period of three years, Dortmund will contribute up to 25 kEuro each for the years 2008 and 2009, the other groups cover the expenses of their engagements.

To achieve these initial goals, we are interested in a larger collaboration with other groups having experience with the readout and tests of the ATLAS pixel chip, the module design and construction, irradiation and evaluation of radiation damage.

Then, for radiation hardness of the electronics, the design needs to be combined with the more advanced CMOS technology discussed above. We invite groups with experience in ASIC design to work on genuine 3D integration ASIC layouts which could then be incorporated into this module concept. Even if real 3D electronic designs can not be achieved within the time scale of the SLHC, integrating the concept of backside contacts with through vias into a single layer of electronics would allow for a much more compact module design than is presently achieved.

R&D item	time		
Technology compatibility	2007		
Production of thin sensors	2007	2008	
SLID thin sensor/pixel chip (no etching)		2008	
Same item with backside etching		2008	
SLID with 3D sensors		2008	
Irradiation and test beam measurements		2008	2009
ICV-SLID (contact with via)			2009
Prototype concept and ICV-ASICs	2007	2008	2009

Table 1: *Time planning for the years 2007-2009.*

R&D item	Bonn	Dortmund	Oslo	Interon	Munich
Test wafer design		x		x	x
Thin sensors production					x
Technology compatibility					x
SLID on thin sensors					x
SLID on 3D sensors			x		x
Pixel chip wafer testing	x				
ASICs for test structures				x	x
Irradiation		x			x
Data evaluation	x	x	x		x
Test beam measurements	x	x	x		x

Table 2: *Matrix of activities of the participating institutes.*

A successfully operated prototype would be a very significant step into the direction of a multi-layer 3D integrated circuit with a silicon sensor as active device. In any case, the novel interconnection process would allow for finer segmentation of hybrid pixel detectors made from thin sensors than what is possible with present technologies.

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